DESIGN, ANALYSIS AND EXPERIMENTAL VERIFICATION OF CENTER-POINT-CLAMPED AC-AC CONVERTER

by

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ABSTRACT

PANKAJ KUMAR BHOWMIK. Design, analysis and experimental verification of Center Point Clamped AC-AC Converter.
(Under the direction of Dr. MADHAV MANJREKAR)

With the increasing use of electronic loads by the consumers, the utilities are facing more and more power quality issues. The advancement in semiconductor industry has led to introduction of power electronic devices as solutions to the power quality issues. But the implementation of these devices at utility scale voltage still remains challenging due to lack of power semiconductor devices rated at utility scale voltages. This thesis proposes a novel topology of power converter that uses semiconductor devices rated at about half the magnitude of utility scale voltage. This novel converter topology would help realizing a power electronic converter for utility scale voltages with easily available semiconductor devices that are rated at half the utility scale voltages.

This thesis investigates a center point clamped ac-ac topology for direct ac-ac power conversion. This converter topology introduces a unique methodology to clamp the voltage to the mid-point of the input transformer thus reducing the voltage blocking requirements on the bi-directional switches employed in such direct ac-ac converter. This thesis also discusses the considerations that are taken into account while designing an input filter for Center-Point-Clamped AC-AC Converter. The switched mode regulators due to their switching action feed in unwanted harmonic currents to the input side. These switching harmonics are attenuated by the designed input filter. But the addition of an input filter changes the transfer functions associated with the converter, which may degrade the performance of the converter and may even destabilize the system. The dynamic analysis of the Center-Point-Clamped AC-AC Converter with an input filter has

been discussed in the thesis. A feedback controller has been designed for closed loop control of the converter. Simulation results presented in the paper verify that the proposed converter offers high power transfer efficiency compared to conventional ac-dc-ac converters, and smaller output voltage ripple along with reduced voltage stress on the bi-directional switches when compared to other direct ac-ac converters. Also, it is seen that the designed input filter reduces the harmonic distortion of the input current, maintains the stability of the system as well as does not degrade the performance of the Center-Point-Clamped AC-AC converter. Experimental results demonstrating the Center-Point-Clamped mechanism of the converter as well as closed loop control of the AC-AC Converter are also presented in the paper.

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LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
IGBT	Integrated Gate Bipolar Transistor
SOA	Safe Operating Area
PWM	Pulse Width Modulation
VeSC	Vector Switching Converter
PACT	Phase Amplitude Controllable Transformer
TACC	Thin AC Converters
SISO	Single Input/Single Output
GUI	Graphical User Interface
EMI	Electro-Magnetic Interference
NI	National Instruments
GPIC	General Purpose Inverter Controller
VI	Virtual Instrument
QML	Query Mark-up Language
MSO	Mixed Signal Oscilloscope
FACTS	Flexible AC Transmission Systems

CHAPTER 1 : INTRODUCTION

1.1. Introduction

This chapter presents a brief introduction and organization of the thesis. Importance of power control equipment to improve power quality is emphasized in Section 1.2. Section 1.3 presents the importance of direct ac-ac converters. Section 1.4 discusses the challenges faced when operating at high voltage and high power levels as well as the primary motivation for the thesis. The concluding section presents organization of the thesis.

1.2. Power Quality Issues in the Modern Utility Grid

Increasing use of loads supplied by electronic power converters in industry has led to growing problems with reliability of the power supply. Computers, adjustable speed drives and automated manufacturing processes are very susceptible to voltage sags, spikes and power interruptions [1], [2]. The need for a reliable and high quality power supply has led to the increased adoption of electronic power conditioning devices and uninterruptible power supplies, which regulate voltages within acceptable tolerances [1], [15]-[17]. Another important issue affecting the modern utility grid is the addition of renewable energy sources to satisfy the surging energy demands. Penetration of renewable energy resources, while critical from the perspective of meeting increasing energy demands, adds to grid congestion and affects system operation [2]. Over the last few decades there has been a growing need for enhanced grid control capabilities

attributed to these issues. Advances in power semiconductor devices have made it possible for utilities to use a variety of power electronics based power control equipment to improve power quality. But the implementation of these power electronic solutions at utility scale voltages remain challenging as semiconductor devices at utility scale voltages are not readily available in the market. Also, these power electronic solutions are costly and less efficient, as they are quite complex. Thus, it may be noted that owing to high cost, complexity and poor reliability these solutions have seen minimal market penetration.

1.3. Comparison of Direct and Indirect AC-AC Converters

The direct ac-ac converter is one of the candidates in realizing a low cost power quality solution with high system reliability [1], [2], [10], [11]. This direct ac-ac conversion is unlike an inverter-based ac-dc-ac converter where additional energy storage is required (in the form of a dc link capacitor). In an indirect ac-ac converter, the power conversion occurs in several stages, like ac power is rectified to dc power and then dc power is inverted to ac power. The intermediate stages in an indirect ac-ac converter involve additional energy storage capacitors. Although such indirect ac-ac converters are simple to control and are cost competitive, they suffer from disadvantages such as requirement of storage element, viz. capacitor, which are bulky in size. Also, the multiple stages in an indirect ac-ac converter often involve a number of active and passive devices, which reduces its efficiency as well as life span. On the other hand, direct ac-ac power converters, without energy storage elements offer advantages such as, single-stage power conversion, superior harmonic content, better efficiency and smaller footprint [2], [10], [11]. Although a number of direct ac-ac converter topologies have been reported in

literature, yet the implementation of these converters at utility scale voltages and power have been a critical issue due to lack of availability of semiconductor devices rated at utility level voltages and power.

1.4. Challenges and Thesis Motivation

Operation of power conditioning systems such as direct ac-ac converters at high voltage and power levels requires semiconductor devices with high voltage blocking and high current carrying capabilities. Commercially available Insulated Gate Bipolar Transistors (IGBTs) rated up to 1700V/1200A that are low cost have been a workhorse for industrial applications operating at 480Vac [2]. These devices operate with relatively high switching frequencies. In order to operate direct ac-ac converter at higher voltage levels in the range of 4.16kV-13.8kV, it requires semiconductor devices rated at those higher voltage levels. As for instance, the phase-neutral peak voltage in a 4.16kV system is 3.4kV. To ensure that devices work reliably within their Safe Operating Area (SOA), it is required to employ either a 6.6kV IGBT or a series connection of two 3.3kV devices for this application. Because of lack of widely available 6.6kV devices, an alternative has been to employ series connection of 3.3kV IGBTs. This increases complexity and cost of system due to issues associated with static and dynamic voltage sharing of series connected IGBTs [2], [18]-[22]. It may be observed that as the voltage ratings of the semiconductor devices increase, the switch on resistance increases, thereby increasing the switching losses and reducing the efficiency of the semiconductor switch based power conditioning devices. An effective solution to all these challenges pertaining to construct a reliable and efficient power conditioning device has been proposed in this thesis in the form of a novel topology of direct ac-ac converter termed as Center-Point-Clamped AC-

AC Direct Power Converter. With the proposed center-point-clamped ac-ac converter topology, it has been shown that one can reliably construct an efficient power conditioning device for utility scale voltage and power ratings using semiconductor devices rated at half the utility scale voltages and power.

1.5. Organization of Thesis

This section presents an overview of the organization of thesis as follows:

Chapter 1: Introduction

This chapter starts by describing the importance of power control equipment to improve power quality in Section 1.2. The advantages of direct ac-ac converters over traditional ac-dc-ac converters are briefly discussed in Section 1.3. The challenges faced at higher voltage and power levels leading to the thesis motivation are discussed in Sections 1.4. The organization of the thesis is presented in Section 1.5.

Chapter 2: Review of AC-AC Direct Power Converters

This chapter presents the evolution of different types of AC-AC Direct Power Converters. A brief overview of the chapter is presented in Section 2.1. The single phase ac chopper circuit with shunt connected bidirectional switches is discussed in Section 2.2. The single phase and three phase ac chopper circuit with shunt and series connected bidirectional switches are studied in Section 2.3. The three phase AC chopper circuit constituting classical model of Pulse Width Modulation (PWM) based converter topologies, viz. buck, boost, and buck-boost converter are analyzed in Section 2.4. The Vector Switching Converter topology for M sources and N loads is discussed in Section 2.5. A generalized model of matrix converter is examined in Section 2.6. The Phase and

Amplitude Controllable Transformer and a multilevel topology of AC-AC converter are studied in Section 2.7 and Section 2.8 respectively.

Chapter 3: Center-Point-Clamped AC-AC Buck Converter

This chapter introduces the novel topology of Center-Point-Clamped AC-AC Buck Converter. The functional capability of Center-Point-Clamped AC-AC Buck Converter is presented in Section 3.1. The working principle of Center-Point-Clamped AC-AC Buck Converter along with its switching sequence is discussed in Section 3.2. The principle of voltage balancing across the input capacitors is analyzed in Section 3.3.

Chapter 4: Circuit Design of Center-Point-Clamped AC-AC Buck Converter

This chapter discusses the circuit design principles followed to derive the various circuit parameters for the Center-Point-Clamped AC-AC Buck Converter. The preface to the chapter is presented in Section 4.1. The simplified circuit schematic of the converter is described in Section 4.2. The design of the converter circuit parameters is analyzed in Section 4.3.

Chapter 5: Dynamic Analysis of Center-Point-Clamped AC-AC Buck Converter

This chapter examines the dynamic analysis of the Center-Point-Clamped AC-AC Buck Converter. A brief overview of the chapter is presented in Section 5.1. The simplified circuit schematic of the converter is described in Section 5.2. The state space equations for the converter are obtained in Section 5.3. The dynamic analysis of the converter transfer functions is presented in Section 5.4.

Chapter 6: Controller Design for closed loop control of Center-Point-Clamped AC-AC Converter

This chapter deals with the design of a feedback controller for closed loop operation of the Center-Point-Clamped AC-AC Buck Converter. The motivation behind this chapter is mentioned in Section 6.1. The simplified circuit schematic of the converter is shown in Section 6.2. The design of the feedback controller has been analyzed in Section 6.3.

Chapter 7: Input Filter considerations for Center-Point-Clamped AC-AC Converter

This chapter examines the considerations that have to be taken care of while designing an input filter for the converter so that the unregulated input side power supply does not get affected due to harmonics generated by the switching action of the converter. A brief preface to the chapter is presented in Section 7.1. The modified simplified circuit schematic of the converter is presented and described in Section 7.2 and Section 7.3. The dynamic analysis of the modified converter circuit is presented in Section 7.4. The considerations for designing the input filter for the converter are analyzed in Section 7.5.

Chapter 8: Simulation Results

This chapter presents the simulation results verifying the efficacy of the Center-Point-Clamped AC-AC Buck Converter. An introduction to the chapter is provided in Section 8.1. The simulation model of the converter is presented in Section 8.2. The waveforms supporting the operating principle of the converter are analyzed in Section 8.3. The open loop and closed loop simulation results are presented in Section 8.4 and Section 8.5 respectively.

Chapter 9: Experimental Results

This chapter discusses the experimental results obtained from a laboratory prototype verifying the practical realization and efficacy of the Center-Point-Clamped AC-AC

Buck Converter. The objective of this chapter is shown in Section 9.1. The experimental set-up is discussed in Section 9.2. The experimental waveforms explaining the operating principle of the converter are presented in Section 9.3. The open loop and closed loop experimental results are presented in Section 9.4 and Section 9.5.

Chapter 10: Family of Center-Point-Clamped AC-AC Converters

This chapter starts by stating the advantages of the family of Center-Point-Clamped AC-AC Direct Power Converter in Section 10.1. The operating principles and the switching methodologies of family of Center-Point-Clamped AC-AC Converters, viz. buck converter, boost converter, buck-boost converter, Ćuk converter are presented in Sections 10.2, 10.3, 10.4, and 10.5 respectively.

Chapter 11: Conclusions

This chapter contains a brief summary of the overall thesis. It also highlights the arguments and solutions presented in the thesis.

CHAPTER 2 : REVIEW OF AC-AC DIRECT POWER CONVERTERS

2.1. Introduction

A brief review of direct ac-ac converters has been presented in the following sections. Although a number of direct ac-ac converters have been reported in literature, selected topologies of converters that are more practical are discussed in the following sections.

2.2. Single Phase Ac Chopper Circuit with Shunt Connected Bidirectional Switches

One of the first appearances of ac chopper circuit can be traced back to 1968 when it was employed for load voltage regulation applications [3]. In this paper, a technique has been introduced, based on forced ignition and extinction of thyristor based switches for ac voltage regulation. A schematic circuit diagram of the proposed technique is shown in figure 2.1.

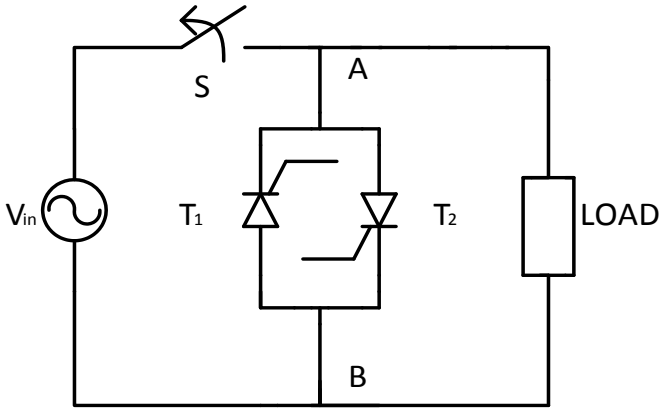


Figure 2.1: Simplified circuit schematic of the single phase of original ac chopper circuit with shunt connected bidirectional switch.

A simplified circuit schematic of one of the earliest known ac chopper circuit has been shown in figure 2.1. It has a switch S which is series with the load. γ is the switching period of the switch S. The switch S is closed during the time interval, θ and opened during the rest of the switching time period, i.e. time interval $\gamma - \theta$. Thus, one cycle of the input voltage may be divided into integral multiples of the switching period. This technique is one of the fundamental PWM based ac voltage regulation applicable in resistive loads. However, it has inherent advantages in case of inductive loads and discontinuous load current as the circuit provides a means to discharge the magnetic energy stored in the inductor. During the half-cycle in which terminal A is at positive potential and S is switched off, thyristor, T_1 is switched on and T_2 is switched off. During the second half-cycle in which terminal B is at positive potential and S is switched on, thyristor, T_2 is switched on and T_1 is switched off. Thus, this methodology enables the prevention of exchange of reactive power between load and source owing to the discharge of magnetic energy near the load. The arrangement of thyristors T_1 and T_2 in back to back configuration acting as bidirectional switches is one of the earliest evidence of ac voltage regulation based on bidirectional switches that has been reported in the literature.

2.3. AC Chopper Circuit with Shunt Connected Bidirectional Switches

Extending the concept of ac voltage regulation further, a combination of shunt and series bidirectional switches realizing a full ac chopper circuit has been reported in [4] for power control applications.

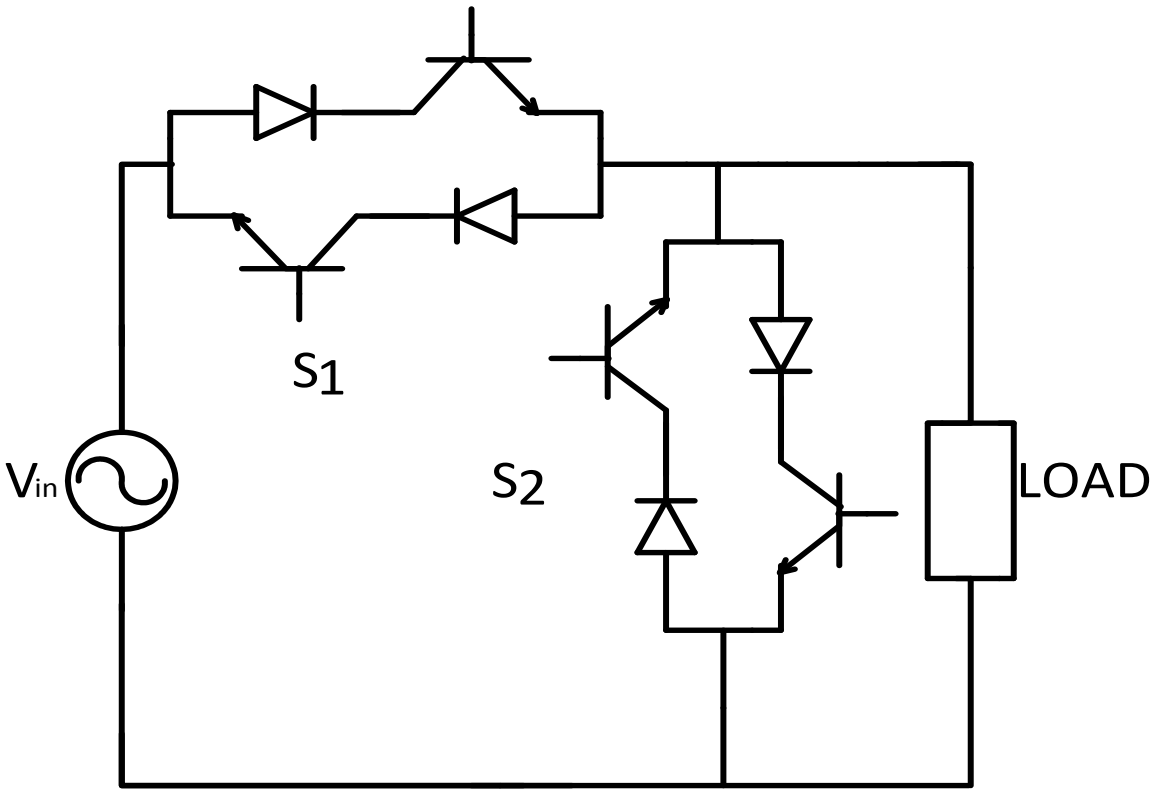


Figure 2.2: Simplified circuit schematic of the single phase of full ac chopper circuit with series and shunt connected bidirectional switches.

The single phase version of ac chopper may be seen in figure 2.2. The bidirectional switches, S_1 and S_2 are closed and opened in a complementary fashion, thereby resulting in chopped ac voltage at the output. The fundamental or rms voltage can be regulated by varying the time ratio, $\tau = t_{on} / (t_{on} + t_{off})$ of the chopping transistors, where t_{on} and t_{off} are the time duration when the switch is closed and opened respectively. In early years, one of the primary hurdles in widespread deployment of this technology was practical realization of a bidirectional switch using Bipolar Junction Transistor (BJT) based devices. A three-phase version of the ac chopper consisted of six bidirectional switches which required twelve BJTs as shown in figure 2.3 [4].

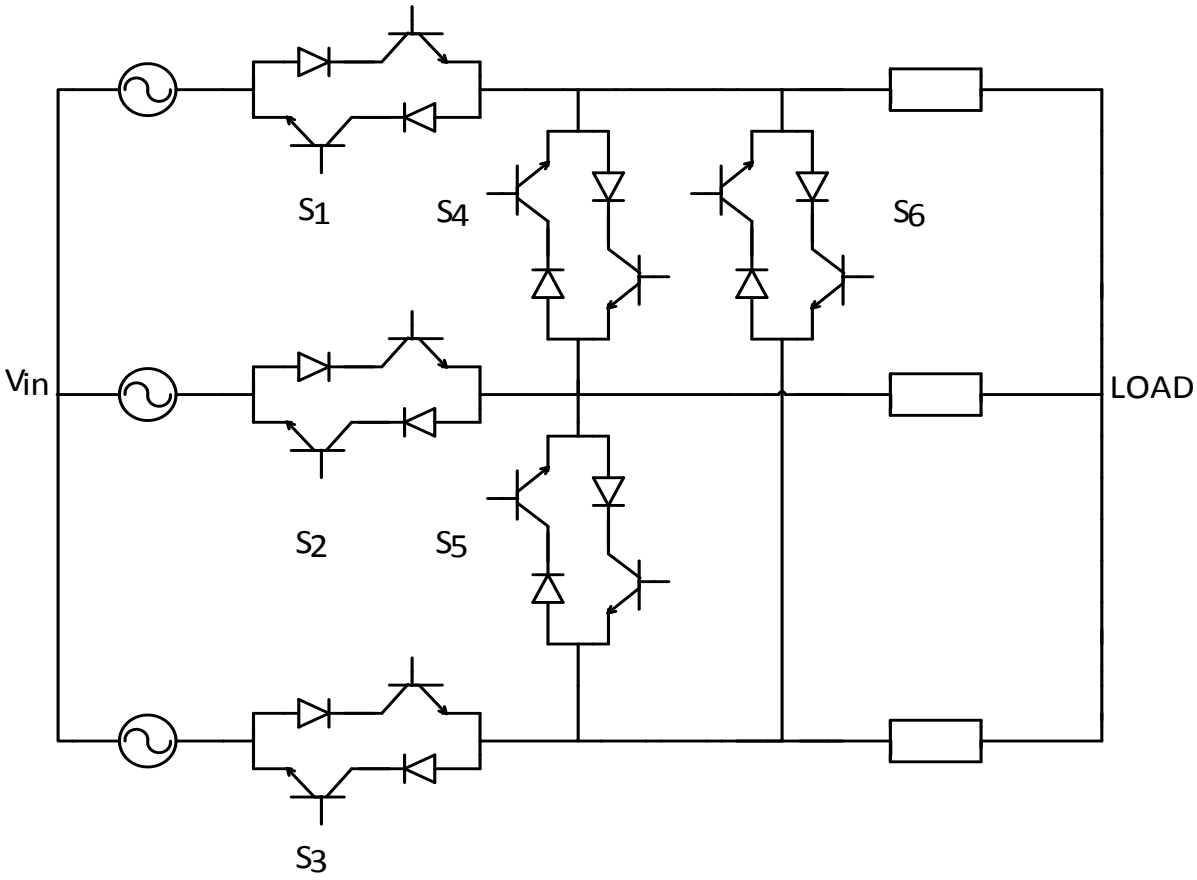


Figure 2.3: Simplified circuit schematic of three-phase AC chopper with six bidirectional switches realized by twelve bipolar junction transistors

The principles of single-phase full ac chopper circuit as in figure 2.2 may be extended to the three phase version as shown in figure 2.3. Since star and delta connected loads are mutually convertible, and the mode of operation is the same in either case, only a star connected load is shown in figure 2.3. The circuit consists of three BJT based bidirectional switches in series and three in shunt. The series switches either act as ac chopping switches in active mode or act as closed switches in the feedback mode. The shunt switches provide a current freewheeling path in active mode or serve as open switches if corresponding line voltage is positive.

2.4. Classical PWM Three Phase AC Chopper Circuit

An equivalent three-phase ac chopper that employed six Integrated Gate Bipolar Transistors (IGBTs) was introduced in [5]. As may be seen from figure 2.4, this topology consists of three floated wye-connected shunt IGBTs which together with their anti-parallel diodes, form bidirectional switches between any two terminals.

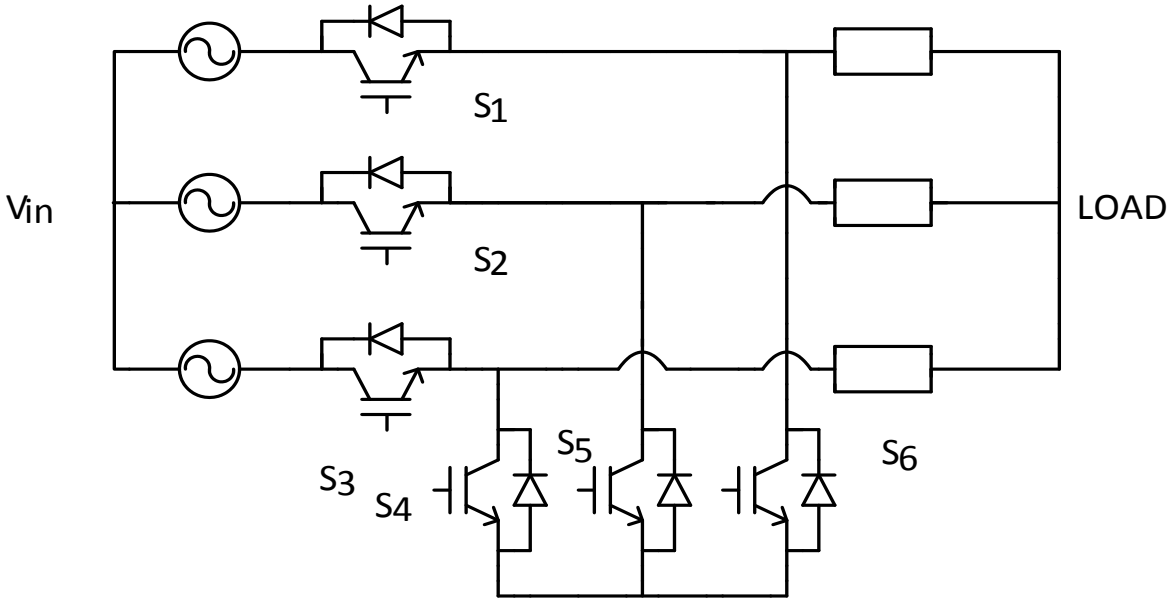


Figure 2.4: Simplified circuit schematic of three-phase AC chopper circuit realized with six insulated gate bipolar transistors.

The three main modes of operation of the ac chopper shown in figure 2.4, are active mode, bypass mode and freewheeling mode. In the active mode of operation, the switches S_1, S_2, and S_3 are closed and the rest are opened. Thus, the input voltages appear across the load, while the three line currents are conducted by one or two top switches (S_1, S_2 and S_3) and two or one diodes antiparallel to top switches. The bypass mode of operation is the transition mode from active mode to freewheeling mode of operation. In this mode, the input and output currents maintain continuity through snubber circuitry (bypass capacitors with parallel bleeding resistors connected in shunt with each line). In the

freewheeling mode of operation, the bottom switches (S_4, S_5 and S_6) are turned on while the rest are turned off. Thus, the three load voltages and the three input line currents are zero, while the three load currents are conducted by one bottom switch and two bottom diodes or vice-versa. The fundamental concept of ac chopper (ac-ac buck converter) topology shown in figure 2.4 can be extended to other forms of switched mode power converters such as boost converter, buck-boost converter, Ćuk converter etc. and has been reported in [6] and [7].

2.5. Vector Switching Converter

The converter shown in figure 2.4 that was originally conceived for a single source, single load system has been further generalized for N sources and M loads with a topology named Vector Switching Converter (VeSC) [8]. A simplified schematic of generalized three-phase VeSC applied to an N source and M load system is shown in figure 2.5.

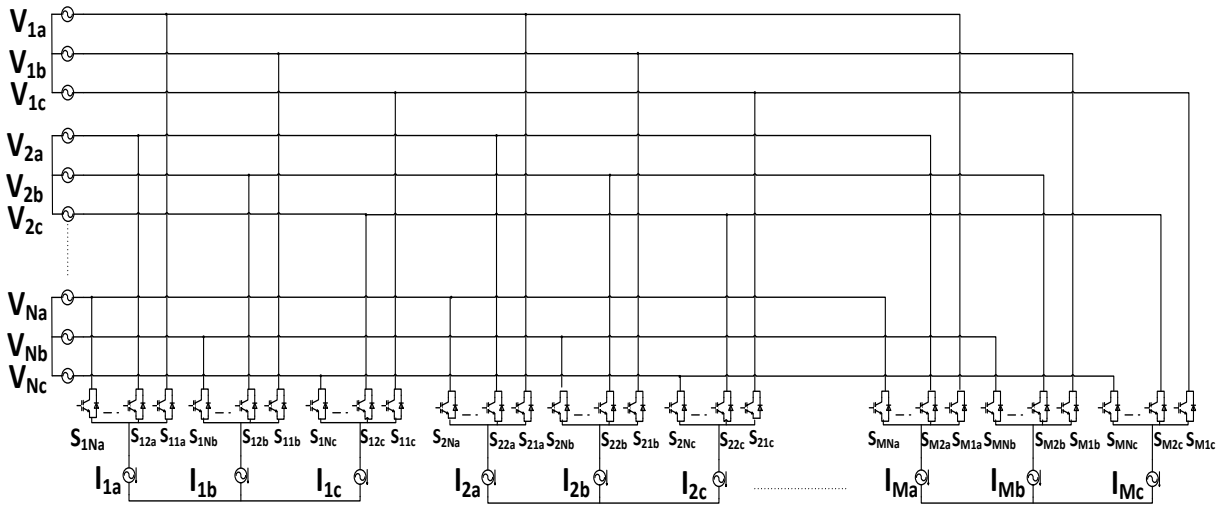


Figure 2.5: Simplified circuit schematic of Vector Switching Converter (VeSC).

As may be seen from figure 2.5, one requires 3xNxM IGBTs to realize a vector switching converter that can interface N stiff three-phase voltage sources with M three-phase loads. The main motivation behind this converter is to regulate the fraction of the power drawn by each three-phase load from each of the three-phase AC sources. It may be observed that the function of each three-pole switch can be seen as selectively connecting the three phase pole current vector to the various three-phase throw voltage vectors, and varying the duty ratio of each throw to modulate the power transfer among them. These converters are termed as Vector Switching Converters, since the working principle of this converter is based on controlling the connectivity between various three-phase AC voltage or current vectors by switching among their components concurrently. It may be noted that a conventional matrix converter would require 9xNxM bidirectional switches or 18xNxM IGBTs for the same purpose [8]. However matrix converter allows significantly higher flexibility in the synthesis of output waveform in terms of its frequency and phase. While as vector switching converters are restricted to power conversion at fundamental frequency and can generate only synchronous voltages, matrix converters are capable of frequency conversion as well as synthesizing voltages that are asynchronous with the source voltage.

2.6. Matrix Converter

With the introduction of matrix converter, research on direct ac-ac power conversion without reactive components received a major boost. The matrix converter [9] has been introduced to obtain sinusoidal waveforms at both input and output ports. It has been used to incorporate bi-directionality in the converter circuit, implement independent control over input and output frequency as well as achieve variable output wave

amplitude and phase. A conventional matrix converter interfacing a three phase voltage source to a three phase load is shown in figure 2.6. It may be observed that it requires 9 bidirectional or 9 IGBTs to realize the matrix converter. Thus, a matrix converter that interfaces N three phase voltage sources to M three phase loads requires 9xNxM bidirectional switches.

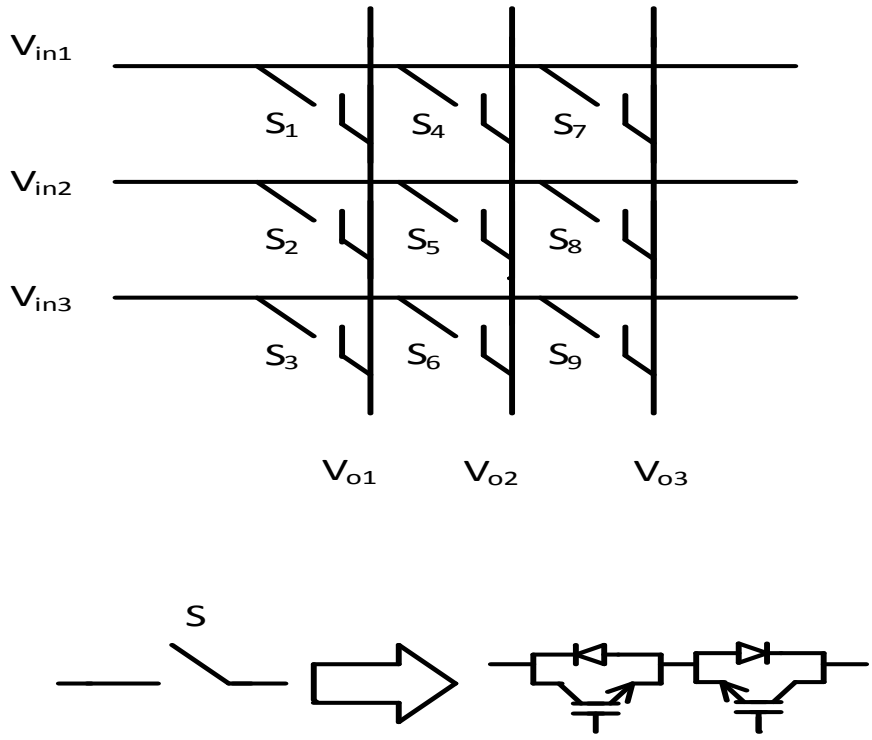


Figure 2.6: Simplified circuit schematic of a three phase to three phase matrix converter

With nine bi-directional switches the matrix converter can theoretically assume 512 (29) different switching states combinations. But not all of them can be usefully employed. Regardless of the control method used, the choice of the matrix converter switching states combinations (also referred as matrix converter configurations) to be used must comply with two basic rules. As the converter is supplied by a voltage source and usually feeds an inductive load, the input phases should not be short-circuited and the output currents should not be interrupted. From a practical point of view these rules imply that one and

only one bi-directional switch per output phase must be switched on at any instant. Taking this constraint into account, there are 27 permitted switching combinations in a three phase to three phase matrix converter. The switching sequence of the matrix converter has been designed such that each output may be fed with a cyclic permutation of the input lines. This cyclic permutation also ensures that if the input three phase system is balanced, the three output phases are naturally equidisplaced.

2.7. Phase and Amplitude Controllable Transformer

The expansion of the applicability of ac choppers beyond voltage amplitude regulation to additional control of phase and frequency of output voltage has been accomplished by the introduction of the concept of dual virtual quadrature sources [10]. Previously, ac-ac direct power converters had been designed to be controlled by traditional duty cycle (varying between 0 and 1). Thus output voltage (V_o) was governed by a simple scalar product of duty ratio (D) and input ac voltage ($V_i \cos\theta$) as shown in equation (1).

$$V_o = D\, V_i \cos\theta \tag{1}$$

By introducing even harmonic terms in the duty ratio, output voltage can contain an additional quadrature component along with odd harmonics as shown in equations (2) and (3).

$$\text{If} \quad D = D_0 + D_2 \sin 2\theta + D_4 \sin 4\theta + D_6 \sin 6\theta + \ldots \tag{2}$$

$$\text{then, } Vo = D_{ref} V_i \cos(\theta+\alpha) + D_3 Vi \sin 3\theta + D_5 Vi \sin 5\theta + \ldots \tag{3}$$

The third harmonic components get trapped in a three-wire system, and thus one can now regulate the phase and frequency content of output voltage to obtain desired fundamental and harmonic reference by controlling the amount of even harmonics introduced in the

duty ratio [10]. An application of the above discussed duty ratio strategy has been shown in the form of a Phase Amplitude Controllable Transformer (PACT).

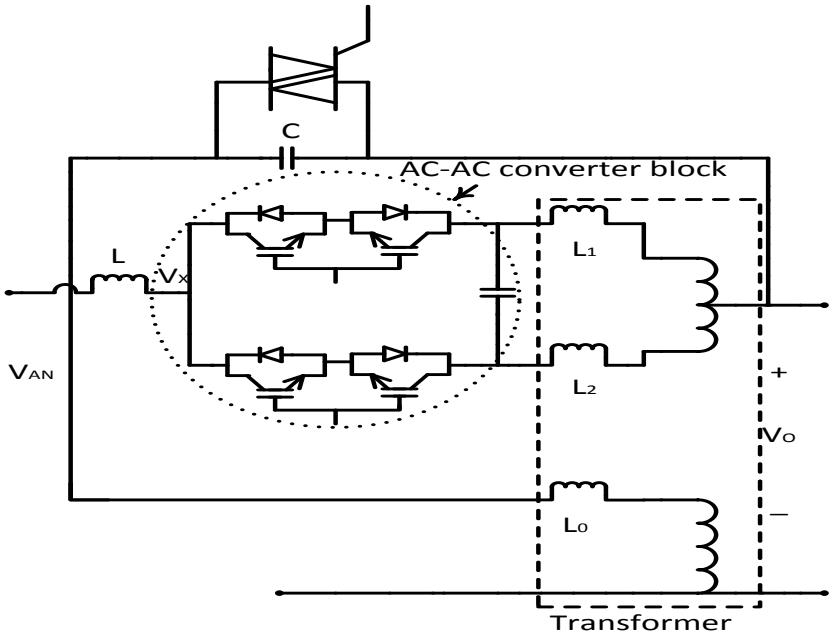


Figure 2.7: Simplified circuit schematic of a Phase Amplitude Controllable Transformer

A circuit schematic of PACT has been shown in figure 2.7. The PACT utilizes the principle of creating dual virtual quadrature sources that facilitates the generation of output voltages with controllable phase and/or harmonic levels without requiring the use of stored energy or additional sources and switches.

2.8. Multilevel Direct AC Converter

The concept of dual quadrature sources based duty ratio control has been extended to build Thin AC Converters (TACC) [2]. This TACC has been used to achieve dynamic control of the grid. Main control objective of TACC is different than inverter or matrix converter, which controlled the output voltage. TACC may be used to reflect modified asset characteristics on the line side, while using the asset within its design specifications.

While the possibility of realizing AC-AC direct power conversion with single devices has been documented extensively in literature, employing this technology to utility scale voltages remains challenging. This is because of the fact that devices such as IGBTs have been predominantly limited to 1700V/1200A for fast switching applications at low cost. Larger devices have now been starting to become commonly available up to 3.3kV, but with slower switching speeds and at higher costs. On the other hand, 6.6kV IGBTs have been more recently introduced and have not been widely available in commercial markets. The ability to series connect these devices reliably has been studied, however it results in further lowering of switching speeds. Although several multilevel dc/ac converter topologies are well known, extending them to direct ac-ac conversion [23]-[27] has not been widely explored. Recently, a topology shown in figure 2.8 has been presented as multilevel ac-ac converter in [11]. Using this multilevel ac-ac converter, TACC can be implemented for higher grid voltages.

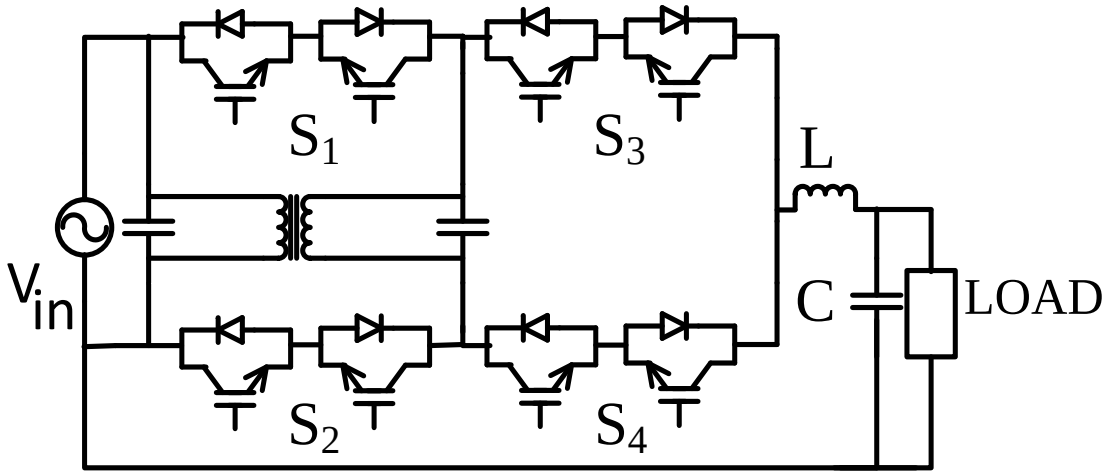


Figure 2.8: Simplified circuit schematic of multilevel ac-ac converter.

As may be seen from figure 2.8, a three-level ac-ac converter is constructed by cascading two ac-ac converters. Topologically similar to the flying capacitor multilevel

dc-ac inverter [12], [24], the goal is to clamp the voltage across each bidirectional switch by an intermediate capacitor. However, one of the challenges associated with this topology is voltage balancing and firm control of this floating capacitor. Hence, a voltage balancing transformer is proposed to mitigate this issue as shown in figure 2.8.

It may be observed from figure 2.8 that the multilevel ac-ac converter topology allows the employment of lower voltage rated IGBTs for building the bidirectional switches, thereby also reducing the switching losses to improve the converter efficiency. But the disadvantage of this converter topology lies in the fact that the number of passive components has increased with the introduction of the voltage balancing transformer. This also has led to significant increase in the size of the converter. Hence one could conclude that the direct ac-ac converters at higher voltages are a challenge to implement, due to lack of higher voltage rated semiconductor devices.

CHAPTER 3 : CENTER-POINT-CLAMPED AC-AC BUCK CONVERTER

3.1. Introduction

This chapter discusses a novel topology for ac-ac direct power conversion that is capable of providing access to the mid-voltage point on the source side. This arrangement offers a means to clamp the voltage across bidirectional switches at half the magnitude of source voltage, thereby allowing employment of low voltage power electronic devices to operate with higher system voltages. Unlike flying capacitor arrangement shown in figure 2.6, the proposed structure requires no transformer for capacitor balancing and follows principle of neutral-point-clamped dc-ac inverter introduced in [13].

Although it is tempting to term the proposed power circuit as an ac-ac 'multilevel' converter, careful examination reveals that contrary to multilevel dc-ac inverter, there are no multiple ac levels which add up to synthesize the output ac voltage. Instead, this converter functions to switch either between full input voltage wave (v_{in}cosθ) and half input voltage wave (v_{in}/2 cosθ), or between half input voltage wave (v_{in}/2 cosθ) and zero(0) to realize the desired output ac voltage waveform. Hence this converter topology is termed as Center-Point-Clamped AC-AC Converter, and not multilevel ac-ac converter.

3.2. Evolution of Center-Point-Clamped AC-AC Converter

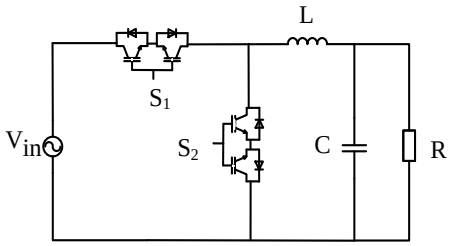


Figure 3.1: Simplified circuit schematics showing single phase ac-ac converter with two bidirectional switches.

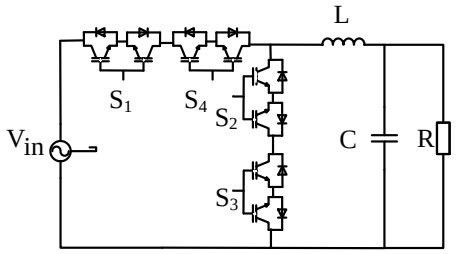


Figure 3.2: Simplified circuit schematics showing single phase ac-ac converter with four bidirectional switches.

This section discusses the evolution of the Center-Point-Clamped AC-AC Converter. Simplified circuit schematic of an ac-ac converter topology with two bi-directional switches, S_1 and S_2 is shown in figure 3.1. The bidirectional switch has been realized by series connection of two back to back insulated gate bipolar transistors (IGBT) with anti-parallel diodes. The bi-directional switches, S_1 and S_2 are operated in a complementary fashion. When switch S_1 is closed, switch S_2 is open, and vice versa. A low pass L-C filter is to filter out the high frequency switching content to get back low frequency ac sinusoid at the output. It may be observed that when switch S_1 is closed, entire input voltage v_{in} is impressed across switch S_2. Similarly, when switch S_2 is closed, voltage across switch S_1 is v_{in}. Thus, maximum voltage stress on switches S_1 and S_2 is the peak of input voltage, v_{in}. In order to employ power devices with limited

blocking voltage capability in a system that exceeds these voltage ratings, one has to resort to series connection of switches.

In this chapter, the design of an ac-ac converter for 4.16kV three-phase distribution system has been discussed. The phase-neutral voltage for a single phase system translates to 2400V ac rms (or 3400V phase-neutral peak voltage) (v_{in}). To ensure that the devices work reliably within their Safe Operating Area (SOA), it is required to employ either a 6.6kV IGBT or a series connection of two 3.3kV devices for this application. As 6.6kV devices are not widely available, our only alternative has been to employ series connection of two 3.3kV IGBTs. This is shown in figure 3.2, where each bidirectional switch is composed of four 3.3KV IGBTs.

An ac-ac converter topology equivalent to the one in figure 3-1(b) is shown in figure 3.3. As may be seen from the simplified schematic of the single phase ac-ac converter in figure 3.3, the four bidirectional switches has been rearranged.

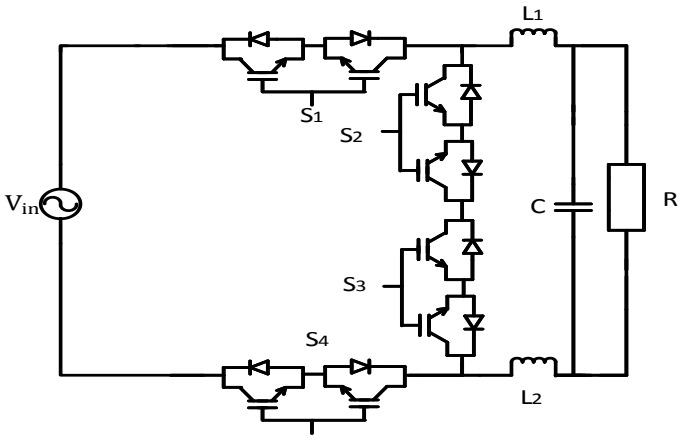


Figure 3.3 Simplified circuit schematic of single phase ac-ac converter.

As is well-known, it is challenging to ensure that the voltages across two series connected devices are distributed evenly during steady state and dynamic conditions. Solving this problem is one of the motivations for this thesis, and the first step towards realizing the Center-Point-Clamped AC-AC Converter topology is rearrangement of four bidirectional devices as shown in figure 3.3 to form a symmetrical converter topology. As may be seen from figure 3.3, the bidirectional switches S_1 and S_4, S_2 and S_3 are series connected to withstand higher voltage ratings at the input. The switches, S_1, S_4, and S_2, S_3 are operated in a complementary manner. When switches S_1 and S_4 are closed, entire input voltage is connected to the load. Whereas when switches S_2 and S_3 are closed, the source is disconnected and load current freewheels. In figure 3.3, inductor (L_1), inductor (L_2) and capacitor (C) are filter components. Load is represented by resistor (R).

3.3. Operating Principle of Center-Point-Clamped AC-AC Buck Converter

In order to achieve even distribution of voltage stresses on the four bidirectional switches under all operating conditions, a center point is constructed on the source side with two capacitors and is tied to the mid-point between switches S_2 and S_3. This center-point provides an access to the midpoint of the input source voltage. Complete circuit of the proposed center point clamped ac-ac converter is shown in figure 3.4. The operating principle of this center-point-clamped ac-ac converter [37] can be thought of as similar to neutral-point-clamped dc-ac inverter [13] in the sense that output can be clamped to the center point of the input.

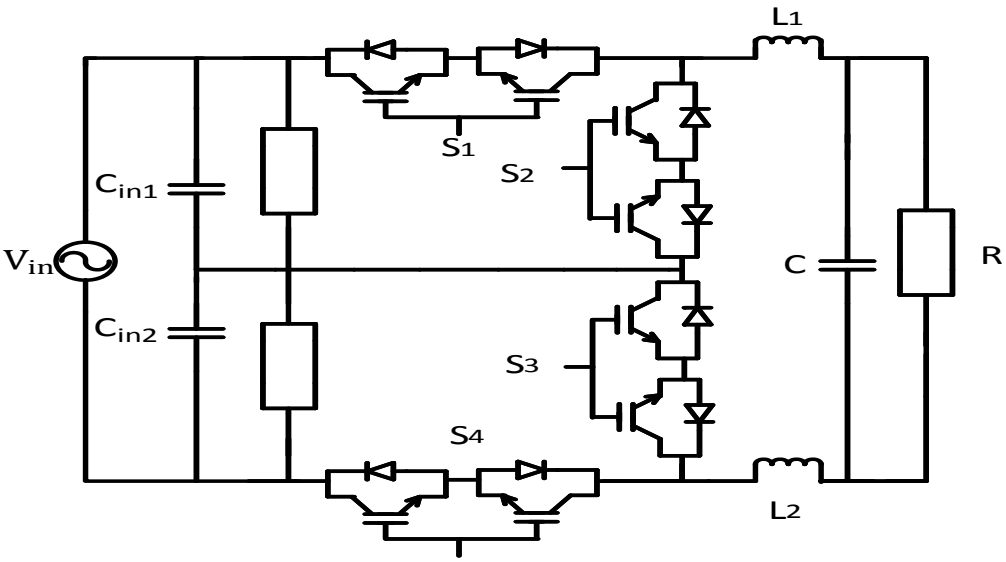


Figure 3.4 Simplified circuit schematic of single phase center point clamped ac-ac converter.

However, instead of generating three 'dc' levels at the pole output ($-V_{dc}/2$, 0, $+V_{dc}/2$) as obtained in a conventional neutral-point-clamped inverter, realizing three distinct 'differential ac' outputs is the key point that distinguishes this topology. It may be observed that when switches S_1, S_4 are closed and switches S_2, S_3 are open, resultant output voltage is equal to input voltage v_{in}. However, because the mid-point between switches S_2 and S_3 is tied to center point on the source, the distribution of voltage between these two open switches S_2 and S_3 is identical and is equal to $v_{in}/2$. Similarly, when switches S_2, S_3 are closed and switches S_1, S_4 are open, the resultant output voltage is zero (0). Again, the distribution of voltage between two open switches S_1 and S_4 is identical and is equal to $v_{in}/2$ because of clamp to the center point. Finally, when switches S_1 and S_3 are closed, the resultant output voltage is half the input voltage i.e. $v_{in}/2$. It may be noted that another combination with switches S_2 and S_4 closed gives the same result of voltage $v_{in}/2$ across the load. However, the difference between these two operating conditions is the capacitor that gets connected to the load. Similar to the

classical neutral-point-clamped dc-ac inverter, these two states are alternately employed so as to evenly balance the voltages across the two capacitors. Switching pattern to generate an ac waveform of desired magnitude at the load side is presented in Table 1.

Table 1. Switching pattern of the proposed center-point-clamped ac-ac converter

Command v_{oref} (desired output)	between 0 and $v_{in}/2$	between $v_{in}/2$ and v_{in}
State 1	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 2	S_2 S_4 closed S_1 S_3 open	S_2 S_4 closed S_1 S_3 open
State 3	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 4	S_1 S_3 closed S_2 S_4 open	S_1 S_3 closed S_2 S_4 open

3.4. Methodology for Balancing Voltages across Input capacitors

One of the unique features of the proposed converter topology is the method to balance input side capacitor voltage for achieving consistent center-point voltage, $v_{in}/2$. As may be seen from Table 1, when switches S_2 and S_3 are closed for zero output voltage level in State 1, capacitors C_{i1} and C_{i2} get equally charged. In order to achieve output voltage $v_{in}/2$ in State 2, switches S_2 and S_4 are closed. This results in discharging of C_{i1} and charging of C_{i2}. For the next zero output voltage level in State 3, switches S_2 and S_3 are closed as in State 1. However, for State 4, instead of S_2 and S_4 for $v_{in}/2$, we close S_1 and S_3. Thus, in this state C_{i2} gets discharged whereas C_{i1} gets charged. This alternate charging and discharging sequence of capacitors C_{i1} and C_{i2} ensures input capacitor voltage balancing. This methodology of capacitor voltage balancing is also applied when the output voltage v_{oref} is regulated from $v_{in}/2$ to v_{in}, as may be seen from Table 1.

CHAPTER 4 : CIRCUIT DESIGN OF CENTER-POINT-CLAMPED AC-AC BUCK CONVERTER

4.1. Introduction

This chapter discusses the design considerations for power circuit design of a center point clamped ac-ac converter. Power circuit design involves determination of the inductance and capacitance values in the converter system. These reactive elements may be represented as functions of inductor ripple current, capacitor ripple voltage and switching frequency. Values of reactive elements are determined using inductor volt-sec balance and capacitor current charge balance methods. Analysis and design methods applied to ac-ac converter are found to be similar to the corresponding dc-dc converter due to their design and functional similarities.

4.2. Circuit Description

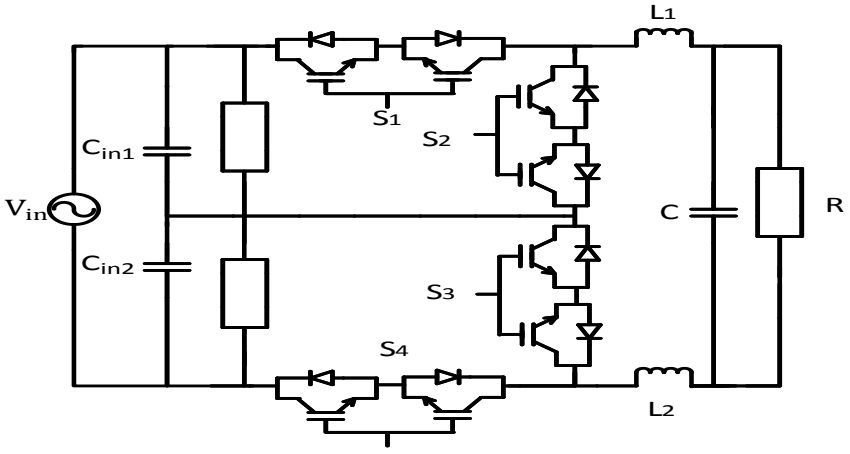


Figure 4.1: Simplified circuit schematic of a single phase of center-point-clamped ac-ac buck converter.

A simplified circuit schematic of a single phase of center-point-clamped ac-ac buck converter is shown in figure 4.1. A representative center-point-clamped ac-ac buck converter is designed for 4.16kV/1MW three-phase application. For a single phase system as shown in figure 4.1, this translates to 2400V ac rms phase-neutral input voltage (or 3400V phase-neutral peak voltage) (v_{in}). The output voltage (v_o) is desired to be set within 10% to 90% of v_{in}. This converter uses 4 bidirectional switches S_1, S_2, S_3, and S_4 which are realized with 8 Insulated Gate Bipolar Transistors (IGBTs) that are switched at 1200Hz (f_{sw}). Filter components include input capacitors C_{i1} and C_{i2}, output inductor (L) and output capacitor (C). R_{Ci1}, R_{Ci2}, R_L and R_C are parasitic resistances associated with these filter components and the load is represented by a resistor R. We neglect the dynamics associated with input filter capacitors C_{i1}, C_{i2}, and their parasitic resistances R_{Ci1} and R_{Ci2}. Hence it is assumed that input voltage is split evenly between the two filter capacitors at any given time.

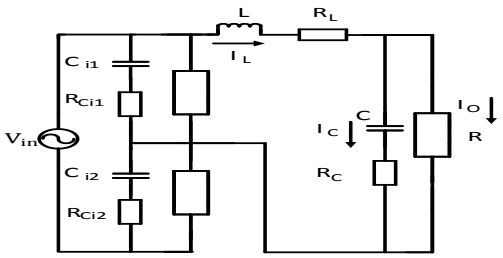
When switches S_1 and S_4 are closed, and switches S_2 and S_3 are open, output voltage is v_{in}. When switches S_1 and S_4 are open, and switches S_2 and S_3 are closed, output voltage is 0. And lastly, when switches S_1 and S_3 (or S_2 and S_4) are closed and switches S_2 and S_4 (or S_1 and S_3) are open, output voltage is $v_{in}/2$. Thus when the desired output voltage is less than 50% of v_{in}, then the converter is switched between 0 and $v_{in}/2$. Whereas, when the desired output voltage is more than 50% of v_{in}, then the converter is switched between $v_{in}/2$ and v_{in}.

4.3. Power Circuit Design

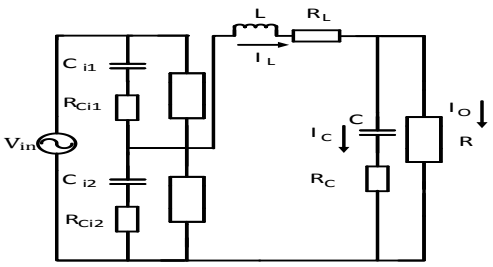
Let us consider 2 regions, in region1 desired output voltage ranges from 0 to $v_{in}/2$, and in region 2 desired output voltage ranges from $v_{in}/2$ to v_{in}.

Region 1: (desired v_o ranges from 0 to v_{in}/2):

Interval T_1 (switches S_1, S_3 (or S_2, S_4) are closed and S_2, S_4 (or S_1, S_3) are open) as shown in figure 4.2.



(a) Switches S_1, S_3 are closed and S_2, S_4 are open.



(b) Switches S_2, S_4 are closed and S_1, S_3 are open.

Figure 4.2: Equivalent circuit of center-point-clamped ac-ac converter in interval T_1.

Applying Kirchoff's voltage laws, we get

$$\frac{v_{in}}{2} - v_L - i_L R_L - v_o = 0 \tag{4.1}$$

Therefore,

$$v_L = \frac{v_{in}}{2} - i_L R_L - v_o \tag{4.2}$$

Current through capacitor,

$$i_c = i_L - \frac{v_o}{R} \tag{4.3}$$

In interval T_2 switches S_2, S_3 are closed and switches S_1, S_4 are open. The equivalent circuit of center point clamped ac-ac converter in interval T_2 is shown in figure 4.3.

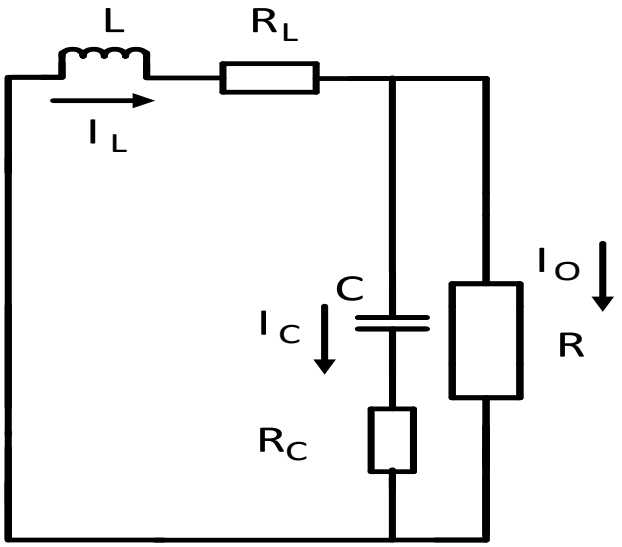


Figure 4.3: Equivalent circuit of center-point-clamped ac-ac converter in interval T_2.

Applying Kirchoff's voltage laws, we get

$$v_L + i_L R_L + v_o = 0 \tag{4.4}$$

Therefore,

$$v_L = -i_L R_L - v_o \tag{4.5}$$

Current through capacitor,

$$i_c = i_L - \frac{v_o}{R} \tag{4.6}$$

Let the time period be T and d be the duty ratio. Thus, dT is the time when switches S_2, S_4 are closed and also when switches S_1, S_3 are closed. For interval T_1, let the duration of operation be $2dT$. In interval T_2, duration of operation will be,

$$T - 2dT = (1 - 2d)T \tag{4.7}$$

$$T = \frac{1}{f_{sw}} \tag{4.8}$$

f_{sw} is the switching frequency.

In steady-state operation, average inductor voltage and average capacitor current over time period T must be zero.

Average inductor voltage,

$$< v_L > = (\frac{v_{in}}{2} - i_L\, R_L - v_o)2d\ + (-i_L\, R_L - v_o)(1 -\ 2d) \tag{4.9}$$

$$(2d)\frac{v_{in}}{2} - v_o - i_L\, R_L = 0 \tag{4.10}$$

Average capacitor current,

$$< i_c > = (i_L - \frac{v_o}{R})2d + (i_L - \frac{v_o}{R})\,(1 - 2d) \tag{4.11}$$

$$i_L - \frac{v_o}{R} = 0 \tag{4.12}$$

Substituting equation (4.12) in (4.10)

$$(2d)\frac{v_{in}}{2} - v_o - (\frac{v_o}{R})\, R_L = 0 \tag{4.13}$$

$$(2d)\frac{v_{in}}{2} - v_o\,(1 + \left(\frac{R_L}{R}\right)) = 0 \tag{4.14}$$

We get,

$$\frac{v_o}{v_{in}} = \frac{d}{(\frac{R_L}{R}+1)} \tag{4.15}$$

Since $R_L << R$,

$$v_0 = d\, v_{in} \tag{4.16}$$

In interval T_1, from equation (4.1),

$R_L << R$, we can neglect the voltage drop across the parasitic resistance of inductor.

So, $v_L = (\frac{v_{in}}{2} - v_o)$ (4.17)

$$L\frac{di_L}{dt} = (\frac{v_{in}}{2} - v_o) \quad (4.18)$$

$$\Delta i_L = \frac{(\frac{v_{in}}{2} - v_o)}{L}(2d)T \quad (4.19)$$

peak to peak $\Delta i_L = \frac{(\frac{v_{in}}{2} - v_o)}{L}(2d)T$ (4.20)

Δi_L is taken as 10% of inductor current $i_{L,}$ we can get i_L, from equation (4.12)

Therefore, $L = \frac{(\frac{v_{in}}{2} - v_o)}{\Delta i_L}(2d)T$ (4.21)

total charge deposited on capacitor plates Q is given by,

$$Q = \Delta v_C C \quad (4.22)$$

Since R_C is negligible, v_C is equal to v_o. Δv_C is taken as 10% of capacitor voltage v_o.

Total charge Q is the area of triangle of Δi_L waveform [13],

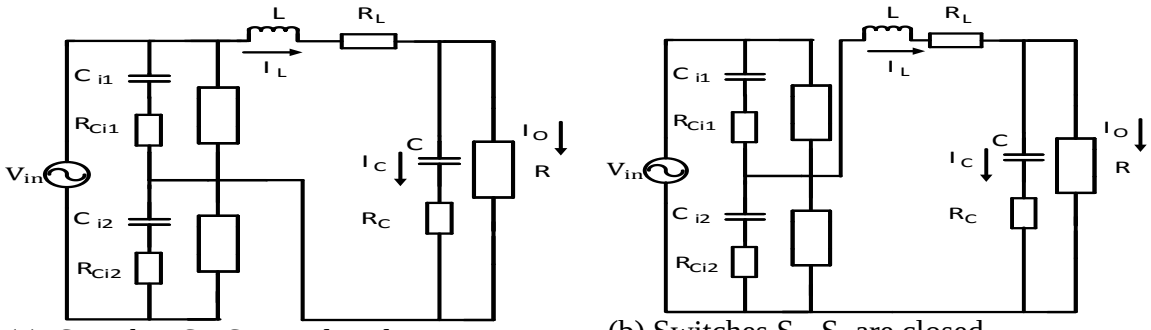
$$Q = \frac{1}{2}\frac{\Delta i_L}{2}\frac{T}{2} \quad (4.23)$$

Substituting equation (4.23) in (4.22)

$$C = \frac{\Delta i_L T}{8\Delta v_C} \quad (4.24)$$

Region 2: (desired v_o ranges from v_{in}/2 to v_{in}):

Interval T_1 (switches $S_{1,}$ S_3 (or $S_{2,}$ S_4) are closed and $S_{2,}$ S_4 (or $S_{1,}$ S_3) are open) as shown in figure 4.4.



(a) Switches S_1, S_3 are closed (b) Switches S_2, S_4 are closed

Figure 4.4: Equivalent circuit of center-point-clamped ac-ac converter in interval T_1.

Applying Kirchoff's voltage laws, we get

$$\frac{v_{in}}{2} - v_L - i_L R_L - v_o = 0 \tag{4.25}$$

Therefore,

$$v_L = \frac{v_{in}}{2} - i_L R_L - v_o \tag{4.26}$$

Current through capacitor,

$$i_c = i_L - \frac{v_o}{R} \tag{4.27}$$

In interval T_2, switches S_2, S_4 are closed and switches S_1, S_3 are open. The equivalent circuit of ac-ac converter in interval T_2 is shown in figure 4.5.

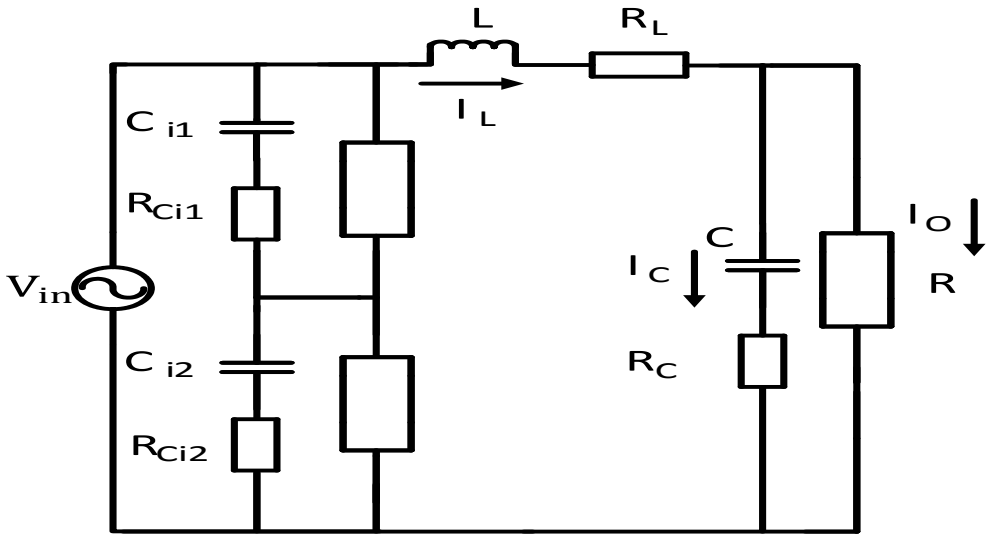


Figure 4.5: Equivalent circuit of center-point-clamped ac-ac converter in interval T_2.

Applying Kirchoff's voltage laws, we get

$$v_{in} - v_L - i_L - v_o = 0 \tag{4.28}$$

Therefore,

$$v_L = v_{in} - i_L R_L - v_o \tag{4.29}$$

Current through capacitor,

$$i_c = i_L - \frac{v_o}{R} \tag{4.30}$$

Let the time period be *T*. *dT* is the time period when switches S_2, S_4 are closed and switches S_1, S_3 are open. In interval T_1, switches S_1, S_3 (or S_2, S_4) are closed and S_2, S_4 (or S_1, S_3) are open,

$$T - dT = (1 - d)T \tag{4.31}$$

$$T = \frac{1}{f_{sw}} \tag{4.32}$$

In steady-state operation, average inductor voltage and average capacitor current over time period T must be zero.

Average inductor voltage

$$< v_L > = \left(\frac{v_{in}}{2} - i_L\, R_L - v_o \right)(1 - d) + (v_{in} - i_L\, R_L - v_o)\, d \tag{4.33}$$

$$(1 + d)\frac{v_{in}}{2} - v_o - i_L\, R_L = 0 \tag{4.34}$$

Average capacitor current,

$$< i_c > = (i_L - \frac{v_o}{R})D + (i_L - \frac{v_o}{R})\,(1 - D) \tag{4.35}$$

$$i_L - \frac{v_o}{R} = 0 \tag{4.36}$$

Substituting equation (4.36) in (4.34)

$$(1 + d)\frac{v_{in}}{2} - v_o - (\frac{v_o}{R})R_L = 0 \tag{4.37}$$

$$(1 + d)\frac{v_{in}}{2} - v_o(1 + \left(\frac{R_L}{R}\right)) = 0 \tag{4.38}$$

$$\frac{V_o}{V_{in}} = \frac{d+1}{2(\frac{R_L}{R}+1)} \tag{4.39}$$

In interval T_2, from equation (4.29),

Since R_L << R, we can neglect the voltage drop across the parasitic resistance of inductor.

So, $v_L = v_{in} - v_o$ (4.40)

$$L\frac{dI_L}{dt} = v_{in} - v_o \quad (4.41)$$

$$\Delta i_L = \frac{v_{in}-v_o}{L}\, dT \quad (4.42)$$

peak to peak $\Delta i_L = \frac{v_{in}-v_o}{L}\, dT$ (4.43)

Δi_L is taken as 10% of inductor current $i_{L.,}$ we can get i_L, from equation (4.36)

Therefore,

$$L = \frac{v_{in}-v_o}{\Delta i_L}\, dT \quad (4.44).$$

Total charge deposited on capacitor plates Q is given by,

$$Q = C\Delta v_C \quad (4.45)$$

Since R_C is negligible, v_C is equal to v_o. Δv_C is taken as 10% of capacitor voltage v_o.

Total charge Q is the area of triangle of Δi_L waveform [13]

$$Q = \frac{1}{2}\frac{\Delta i_L}{2}\frac{T}{2} \quad (4.46)$$

Substituting equation (4.46) in (4.45)

$$C = \frac{\Delta i_L T}{8\Delta v_C} \quad (4.47)$$

Substituting values of v_o, v_{in}, d, T, Δi_L, Δv_C in equations (4.21), (4.24) (4.44), (4.47), we can get inductance and capacitance values as shown in Table 2.

Table 4.1 Inductance and capacitance values of CENTER-POINT-CLAMPED ac-ac converter.

	Desired v_o	*D*	*L*	*C*
Region1	0.1 v_{in}	0.1	2.3 mH	300 µF
	0.4 v_{in}	0.4	9.25 mH	18.8 µF
Region 2	0.6 v_{in}	0.2	13.8 mH	8.34 µF
	0.9 v_{in}	0.8	20.8 mH	3.71 µF

For L > 20.8 mH, the converter enters the discontinuous conduction mode and for L < 20.8 mH, the converter cannot operate in region 2, for v_{ref} = 0.9 v_{in} . For C < 300 µF, the converter cannot operate in region 1, v_{ref} = 0.1 v_{in}. So we select output filter components values in such a way that the converter can operate in both regions 1 and 2.

Therefore, output filter components values are,

L = 20.8 mH

C = 300 µF

CHAPTER 5 : DYNAMIC ANALYSIS OF CENTER-POINT-CLAMPED AC-AC BUCK CONVERTER

5.1. Introduction

In this chapter using a state space modelling and an average technique, transfer functions G_d (transfer function between the output voltage to duty ratio) and G_v (transfer function between the output voltage to input voltage) for the center point clamped ac-ac converter are derived. Frequency response of the system is evaluated using transfer functions G_v and G_d.

5.2. Circuit Description

A simplified circuit schematic of a single phase of center-point-clamped ac-ac converter is shown in Figure 5.1.

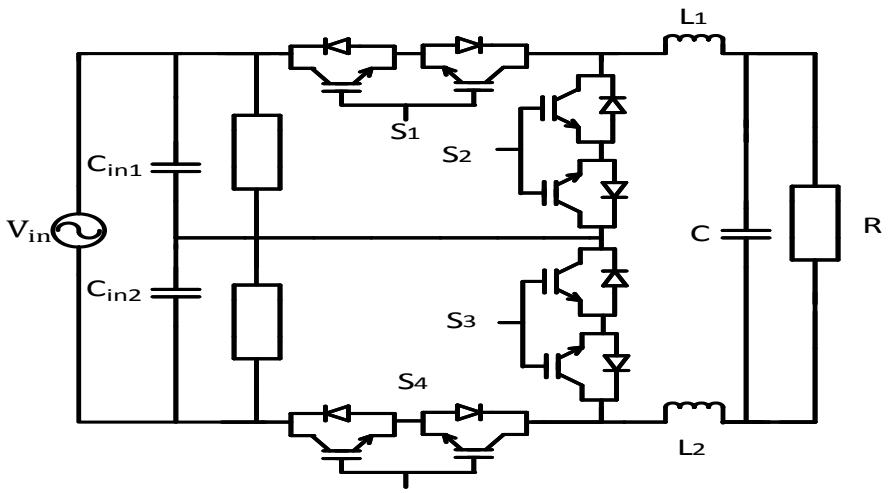


Figure 5.1: Simplified circuit schematic of a single phase of center-point-clamped ac-ac buck converter.

A representative center-point-clamped ac-ac buck converter circuit description is same as given in chapter 4.

5.3. State Space Equations

State space equations for a generic switched circuit that is operated in two intervals T_1 and T_2 are given by:

I. Interval T_1 (operating for duration dT in a given time period T)

$$\dot{x} = A_1 x + b_1 u \tag{5.1}$$

II. Interval T_2 (operating for duration $(1–d)T$ in a given time period T)

$$\dot{x} = A_2 x + b_2 u \tag{5.3}$$

$$y = c_2^T x \tag{5.4}$$

where x is the state of the system, u is the input, and y is the output [14]

State space equations in interval T_1 can be expressed with reference to d as:

$$\dot{x} = (A_1 x + b_1 u)\, d \tag{5.5}$$

State space equations in interval T_2 can be expressed with reference to $(1–d)$ as:

$$\dot{x} = (A_2 x + b_2 u)(1 - d) \tag{5.7}$$

$$y = c_2^T x(1 - d) \tag{5.8}$$

Averaging both sets of equations for the two switched intervals we get

$$\dot{x} = d(A_1 x + b_1 u) + (1 - d)(A_2 x + b_2 u) \tag{5.9}$$

$$y = d c_1^T x + (1 - d) c_2^T x \tag{5.10}$$

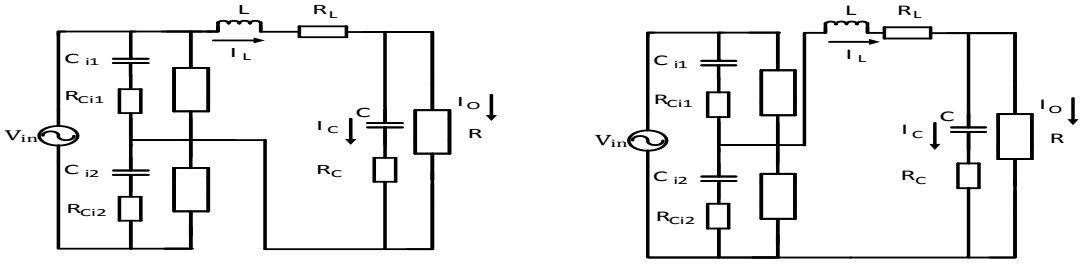
5.4. Dynamic Analysis

For the center-point-clamped ac-ac buck converter circuit shown in Figure 5.1, state variables are inductor current, i_L, and capacitor voltage, v_c. Input is input voltage v_{in}, and output is output voltage v_o

Let us consider 2 regions, in region 1 desired output voltage ranges from 0 to $v_{in}/2$, and in region 2 desired output voltage ranges from $v_{in}/2$ to v_{in}.

Region 1: (desired v_o ranges from 0 to $v_{in}/2$):

Interval T_1 (switches S_1, S_3 (or S_2, S_4) are closed and S_2, S_4 (or S_1, S_3) are open) as shown in Figure 5.2.



(a) Switches S_1, S_3 are closed and S_2, S_4 are open.

(b) Switches S_2, S_4 are closed and S_1, S_3 are open.

Figure 5.2: Equivalent circuits of a center-point-clamped ac-ac converter in interval T_1.

Applying Kirchoff's voltage laws, we get

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c(i_L - i_o) + v_c \tag{5.11}$$

$$v_c = (i_o - i_L)R_c + i_o R \tag{5.12}$$

Rearranging equation 5.12,

$$i_o = \frac{v_c + i_L R_c}{R_c + R} \tag{5.13}$$

Substituting i_o in equation 5.11,

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) + v_c \tag{5.14}$$

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{-v_c + i_L R}{R_c + R}\right) + v_c \tag{5.15}$$

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{i_L R}{R_c + R}\right) - R_c\left(\frac{v_c}{R_c + R}\right) + v_c \tag{5.16}$$

$$\frac{v_{in}}{2} = i_L(R_L + R||R_c) + L\frac{di_L}{dt} + R\left(\frac{v_c}{R_c + R}\right) \tag{5.17}$$

Thus, state equation for i_L is,

$$\frac{di_L}{dt} = -\frac{(R_L + (R||R_c))}{L} i_L - \frac{R}{(R + R_c)L} v_c + \frac{1}{2L} v_{in} \tag{5.18}$$

Applying Kirchoff's current law, we get

$$(i_L - i_o) = C\frac{dv_c}{dt} \tag{5.19}$$

Substituting i_o in equation 5.19,

$$\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) = C\frac{dv_c}{dt} \tag{5.20}$$

Thus, state equation for v_c is,

$$\frac{dv_c}{dt} = \frac{R}{(R + R_c)C} i_L - \frac{1}{(R + R_c)C} v_c \tag{5.21}$$

We can combine equations 5.18 and 5.21 to give

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} v_{in} \tag{5.22}$$

Finally, output equation for v_o is,

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.23}$$

Interval T_2 (switches S_1, S_4 are open and switches S_2, S_3 are closed) as shown in figure 5.3:

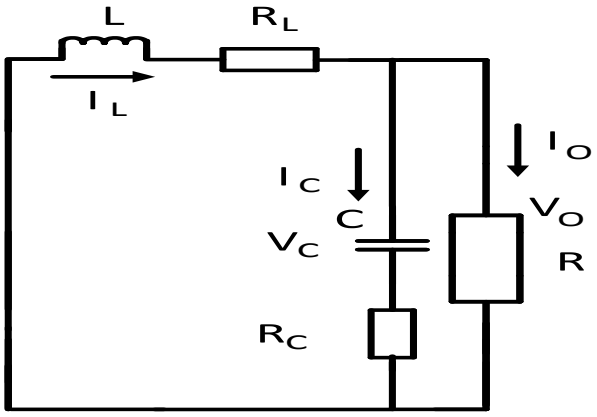


Figure 5.3: Equivalent circuit of a center-point-clamped ac-ac converter in interval T_2.

Applying Kirchoff's voltage laws, we get

$$0 = i_L R_L + L\frac{di_L}{dt} + R_c(i_L - i_o) + v_c \tag{5.24}$$

$$v_c = (i_o - i_L)R_c + i_o R \tag{5.25}$$

Rearranging equation 5.25,

$$i_o = \frac{v_c + i_L R_c}{R_c + R} \tag{5.26}$$

Substituting i_o in equation 5.24,

$$0 = i_L R_L + L\frac{di_L}{dt} + R_c\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) + v_c \tag{5.27}$$

$$0 = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{-v_c + i_L R}{R_c + R}\right) + v_c \tag{5.28}$$

$$0 = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{i_L R}{R_c + R}\right) - R_c\left(\frac{v_c}{R_c + R}\right) + v_c \tag{5.29}$$

$$0 = i_L(R_L + R||R_c) + L\frac{di_L}{dt} + R\left(\frac{v_c}{R_c + R}\right) \tag{5.30}$$

Thus, state equation for i_L is,

$$\frac{di_L}{dt} = -\frac{(R_L + (R||R_c))}{L}\, i_L - \frac{R}{(R + R_c)L} v_c \tag{5.31}$$

Applying Kirchoff's current law, we get

$$(i_L - i_o) = C\frac{dv_c}{dt} \tag{5.32}$$

Substituting i_o in equation 5.32,

$$\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) = C\frac{dv_c}{dt} \tag{5.33}$$

Thus, state equation for v_c is,

$$\frac{dv_c}{dt} = \frac{R}{(R + R_c)C} i_L - \frac{1}{(R + R_c)C}\, v_c \tag{5.34}$$

We can combine equations 5.31 and 5.34 to give

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{in} \tag{5.35}$$

Finally, output equation for v_o is,

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.36}$$

Thus, from equations 5.22 and 5.23, we get

$$A_1 = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.37}$$

$$b_1 = \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} \tag{5.38}$$

$$c_1^T = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \tag{5.39}$$

And, from equations 5.35 and 5.36, we get

$$A_2 = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.40}$$

$$b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{5.41}$$

$$c_2^T = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \tag{5.42}$$

Finally, from equations 5.9 and 5.10, we obtain the matrices

$$A = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.43}$$

$$b = \begin{bmatrix} \frac{d}{2L} \\ 0 \end{bmatrix} \tag{5.44}$$

$$c^T = \begin{bmatrix} (R_c \,||R) & \frac{R}{R+R_c} \end{bmatrix} \tag{5.45}$$

Thus the dynamic equations for the center-point-clamped ac-ac buck converter system for Region 1 are:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d}{2L} \\ 0 \end{bmatrix} v_{in} \tag{5.46}$$

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.47}$$

Now let us introduce a perturbation in input voltage (*u*) and duty ratio (*d*) causing a corresponding perturbation in state variables (*x*) and output (*y*).

$$x = X + \hat{x} \tag{5.48}$$

$$y = Y + \hat{y} \tag{5.49}$$

$$u = U + \hat{u} \tag{5.50}$$

$$d = D + \hat{d} \tag{5.51}$$

Substituting in equations 5.46 and 5.47,

$$\begin{bmatrix} \frac{dI_L}{dt} + \frac{d\hat{\imath}_L}{dt} \\ \frac{dV_c}{dt} + \frac{d\hat{v}_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} I_L + \hat{\imath}_L \\ V_c + \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D+\hat{d}}{2L} \\ 0 \end{bmatrix} (V_{in} + \hat{v}_{in}) \tag{5.52}$$

$$[v_o + \hat{v}_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} I_L + \hat{\imath}_L \\ V_c + \hat{v}_C \end{bmatrix} \tag{5.53}$$

But, from equations 5.46 and 5.47,

$$\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{D}{2L} \\ 0 \end{bmatrix} V_{in} \tag{5.54}$$

$$[V_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} \tag{5.55}$$

Thus subtracting equation 5.54 from 5.52, and equation 5.55 from 5.53, we get

$$\begin{bmatrix} \frac{d\hat{\imath}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} \hat{\imath}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{\hat{d}}{2L} \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} \frac{D}{2L} \\ 0 \end{bmatrix} \hat{v}_{in} \tag{5.56}$$

$$[\hat{v}_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} \hat{\imath}_L \\ \hat{v}_C \end{bmatrix} \tag{5.57}$$

Transforming equation (5.56) to Laplace domain we get,

$$sL\hat{\imath}_L(s) = -(R_L + R \,||\, R_C)\hat{\imath}_L(s) - \frac{R}{(R+R_C)}\hat{v}_C(s) + \frac{D}{2}\hat{v}_{in}(s) + \frac{V_{in}}{2}\hat{d}(s) \tag{5.58}$$

$$sC\hat{v}_C(s) = \frac{R}{R+R_C}\hat{\imath}_L(s) - \frac{1}{R+R_C}\hat{v}_C(s) \tag{5.59}$$

Rearranging,

$$(sC + \frac{1}{R+R_C})\widehat{v_C}(s) = \frac{R}{R+R_C}\widehat{\imath_L}(s) \tag{5.60}$$

$$(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{\imath_L}(s) \tag{5.61}$$

Similarly, transforming output equation (5.57) to Laplace domain we get

$$\widehat{v_o}(s) = (R \,||\, R_C\,)\widehat{\imath_L}(s) + \frac{R}{(R+R_C)}\widehat{v_C}(s) \tag{5.62}$$

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) - R_C\widehat{\imath_L}(s) = \widehat{v_C}(s) \tag{5.63}$$

Substituting from equation (5.61),

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) - R_C(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{v_C}(s) \tag{5.64}$$

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) = R_C\left(sC\left(\frac{R+R_C}{R}\right) + \frac{1}{R}\right)\widehat{v_C}(s) + \widehat{v_C}(s) \tag{5.65}$$

$$\widehat{v_o}(s) = R_C\left(sC + \frac{1}{R+R_C}\right)\widehat{v_C}(s) + \left(\frac{R}{R+R_C}\right)\widehat{v_C}(s) \tag{5.66}$$

$$\widehat{v_o}(s) = sR_CC\,\widehat{v_C}(s) + \widehat{v_C}(s) \tag{5.67}$$

$$\widehat{v_o}(s) = (1 + sR_CC)\,\widehat{v_C}(s) \tag{5.68}$$

Substituting in equation (5.61),

$$(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{\imath_L}(s) \tag{5.69}$$

$$\frac{1}{1+sR_CC}(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_o}(s) = \widehat{\imath_L}(s) \tag{5.70}$$

Substituting in equation (5.58),

$$sL\frac{1}{1+sR_CC}\left(sC\left(\frac{R+R_C}{R}\right)+\frac{1}{R}\right)\widehat{v_o}(s)=-(R_L+R\,||\,R_C)\frac{1}{1+sR_CC}\left(sC\left(\frac{R+R_C}{R}\right)+\frac{1}{R}\right)\widehat{v_o}(s)-\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)+\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.71)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\,\widehat{v_o}(s)=-(R_L+R\,||\,R_C)\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\,\widehat{v_o}(s)-\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)+\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.72)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\,\widehat{v_o}(s)+(R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\,\widehat{v_o}(s)+\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)=\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.73)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{R}\,\widehat{v_o}(s)+(R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}\,\widehat{v_o}(s)+\frac{R}{(R+R_C)}\widehat{v_o}(s)=(1+sR_CC)(\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)) \quad (5.74)$$

$$(sL+R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}\,\widehat{v_o}(s)+\frac{R}{(R+R_C)}\widehat{v_o}(s)=(1+sR_CC)(\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)) \quad (5.75)$$

$$[(sL+R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}+\frac{R}{(R+R_C)}]\widehat{v_o}(s)=(1+sR_CC)(\frac{D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)) \quad (5.76)$$

From equation (5.76), we get transfer functions as,

$$G_d=\frac{\widehat{v_o}(s)}{\hat{d}(s)}_{\widehat{v_{in}}(s)=0} \quad (5.77)$$

$$G_v=\frac{\widehat{v_o}(s)}{\widehat{v_{in}}(s)}_{\hat{d}(s)=0} \quad (5.78)$$

where G_d is the transfer function between the output voltage to duty ratio and G_v is the transfer function between the output voltage to input voltage.

Substituting equation (5.76) in (5.77) and (5.78), we obtain,

$$G_d = \frac{V_{in}}{2([\left(\frac{Cs\left(\frac{R+R_C}{R}\right)+\frac{1}{R}}{1+sCR_C}\right)(Ls+ R_L+R\ ||R_C\ )]+\frac{R}{(R+R_C)})} \tag{5.79}$$

$$G_v = \frac{D}{2([\left(\frac{Cs\left(\frac{R+R_C}{R}\right)+\frac{1}{R}}{1+sCR_C}\right)(Ls+ R_L+R\ ||R_C\ )]+\frac{R}{(R+R_C)})} \tag{5.80}$$

For desired output voltage (0 to v_{in}/2):

Transfer functions G_d and G_v are given by equations (5.79) and (5.80). Uncompensated bode plots of equation (5.79) and equation (5.80) are shown in Figure (5.4) and Figure (5.5),

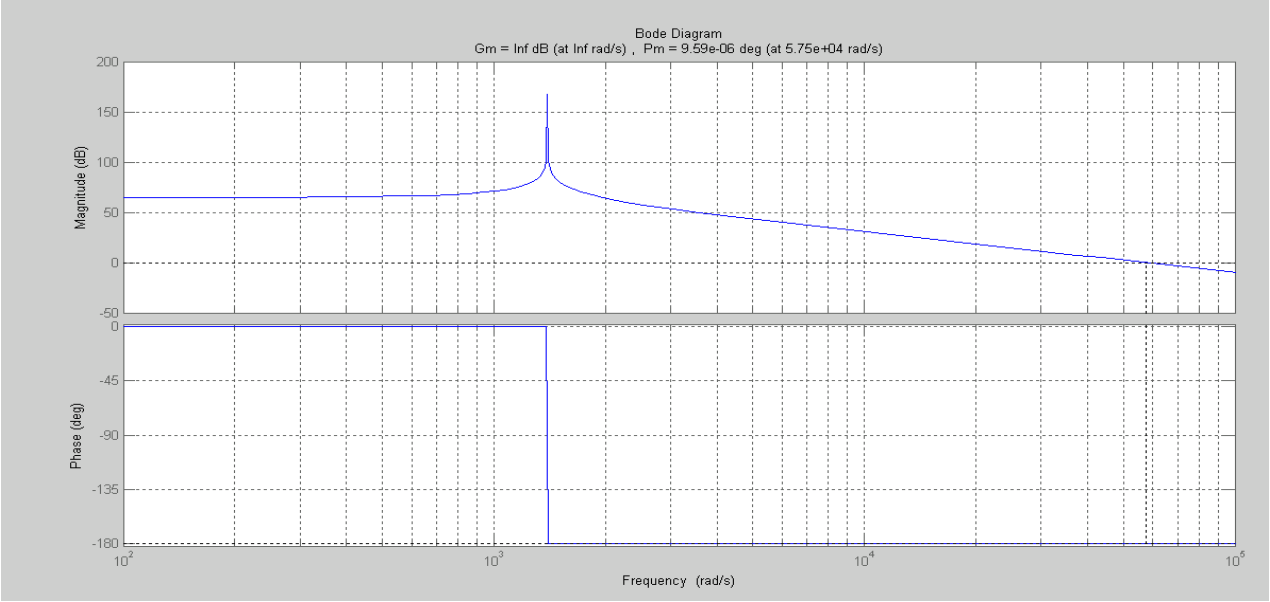


Figure 5.4: Magnitude and phase plots of transfer function G_d for output voltage range 0 to v_{in}/2.

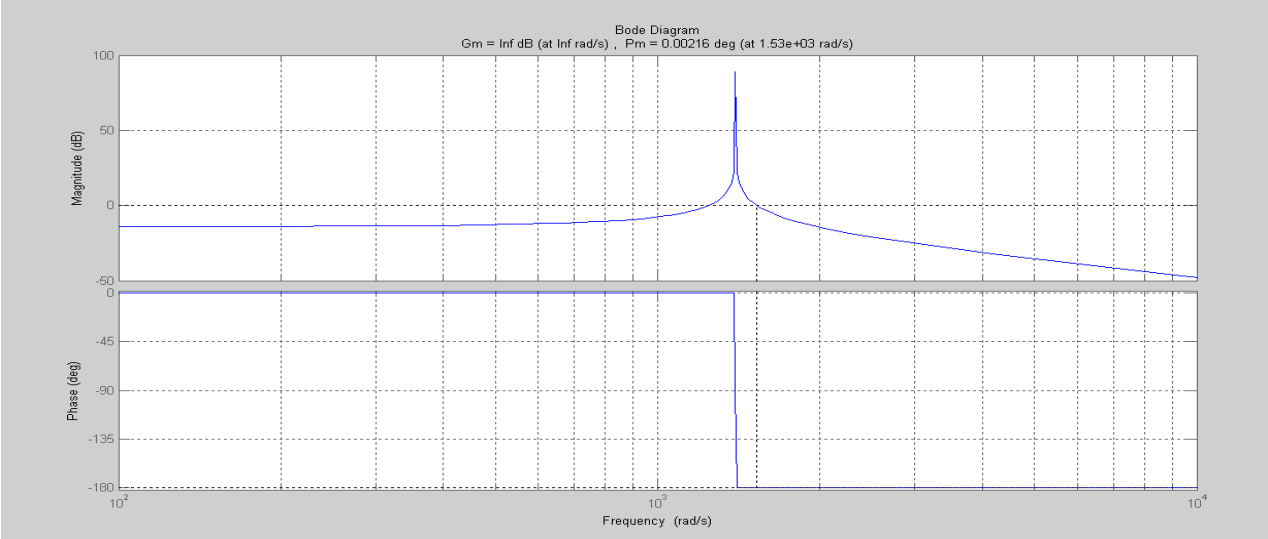


Figure 5.5: Magnitude and phase plots of transfer function G_v for output voltage range 0 to $v_{in}/2$.

Region 2: (desired v_o ranges from $v_{in}/2$ to v_{in}):

Interval T_1 (switches S_1, S_4 are closed and switches S_2, S_3 are open) as shown in figure 5.6

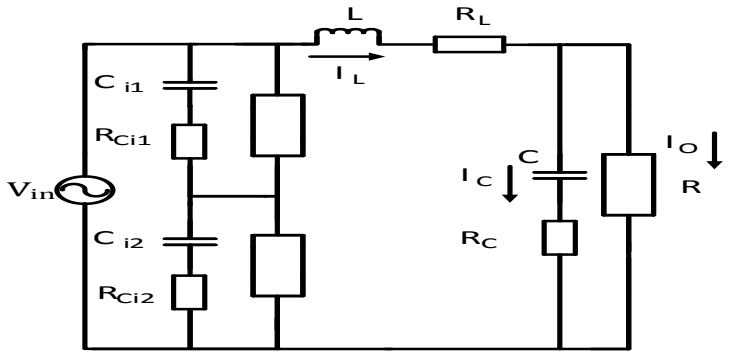


Figure 5.6: Equivalent circuit of a center-point-clamped ac-ac buck converter in interval T_1.

Applying Kirchoff's voltage laws, we get

$$v_{in} = i_L R_L + L\frac{di_L}{dt} + R_c(i_L - i_o) + v_c \tag{5.81}$$

$$v_c = (i_o - i_L)R_c + i_o R \tag{5.82}$$

Rearranging equation 5.82,

$$i_o = \frac{v_c + i_L R_c}{R_c + R} \tag{5.83}$$

Substituting i_o in equation 5.81,

$$v_{in} = i_L R_L + L\frac{di_L}{dt} + R_c\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) + v_c \tag{5.84}$$

$$v_{in} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{-v_c + i_L R}{R_c + R}\right) + v_c \tag{5.85}$$

$$v_{in} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{i_L R}{R_c + R}\right) - R_c\left(\frac{v_c}{R_c + R}\right) + v_c \tag{5.86}$$

$$v_{in} = i_L(R_L + R||R_c) + L\frac{di_L}{dt} + R\left(\frac{v_c}{R_c + R}\right) \tag{5.87}$$

Thus, state equation for i_L is,

$$\frac{di_L}{dt} = -\frac{(R_L + (R||R_c))}{L} i_L - \frac{R}{(R + R_c)L} v_c + \frac{1}{L} v_{in} \tag{5.88}$$

Applying Kirchoff's current law, we get

$$(i_L - i_o) = C\frac{dv_c}{dt} \tag{5.89}$$

Substituting i_o in equation 5.89,

$$\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) = C\frac{dv_c}{dt} \tag{5.92}$$

Thus, state equation for v_c is,

$$\frac{dv_c}{dt} = \frac{R}{(R + R_c)C} i_L - \frac{1}{(R + R_c)C} v_c \tag{5.93}$$

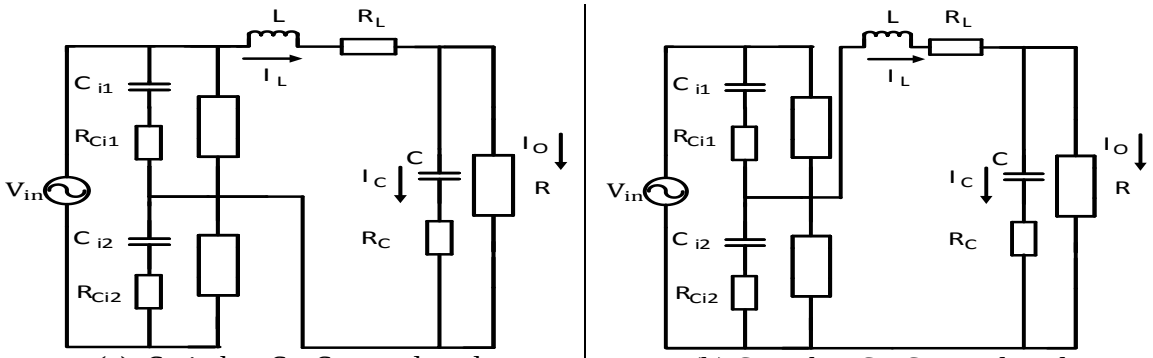
We can combine equations 5.88 and 5.93 to give

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in} \tag{5.94}$$

Finally, output equation for v_o is,

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.95}$$

Interval T_2 (switches S_1, S_3 (or S_2, S_4) are closed and S_2, S_4 (or S_1, S_3) are open) as shown in figure 5.7.



(a) Switches S_1, S_3 are closed (b) Switches S_2, S_4 are closed

Figure 5.7: Equivalent circuits of a center-point-clamped ac-ac buck converter in interval T_2.

Applying Kirchoff's voltage laws, we get

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c(i_L - i_o) + v_c \tag{5.96}$$

$$v_c = (i_o - i_L)R_c + i_o R \tag{5.97}$$

Rearranging equation 5.97,

$$i_o = \frac{v_c + i_L R_c}{R_c + R} \tag{5.98}$$

Substituting i_o in equation 5.96,

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) + v_c \tag{5.99}$$

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{-v_c + i_L R}{R_c + R}\right) + v_c \tag{5.100}$$

$$\frac{v_{in}}{2} = i_L R_L + L\frac{di_L}{dt} + R_c\left(\frac{i_L R}{R_c + R}\right) - R_c\left(\frac{v_c}{R_c + R}\right) + v_c \tag{5.101}$$

$$\frac{v_{in}}{2} = i_L(R_L + R||R_c) + L\frac{di_L}{dt} + R\left(\frac{v_c}{R_c + R}\right) \tag{5.102}$$

Thus, state equation for i_L is,

$$\frac{di_L}{dt} = -\frac{(R_L + (R||R_c))}{L} i_L - \frac{R}{(R + R_c)L} v_c + \frac{1}{2L} v_{in} \tag{5.103}$$

Applying Kirchoff's current law, we get

$$(i_L - i_o) = C\frac{dv_c}{dt} \tag{5.104}$$

Substituting i_o in equation 5.104,

$$\left(i_L - \frac{v_c + i_L R_c}{R_c + R}\right) = C\frac{dv_c}{dt} \tag{5.105}$$

Thus, state equation for v_c is,

$$\frac{dv_c}{dt} = \frac{R}{(R + R_c)C} i_L - \frac{1}{(R + R_c)C} v_c \tag{5.106}$$

We can combine equations 5.103 and 5.106 to give

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} v_{in} \tag{5.107}$$

Finally, output equation for v_o is,

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.108}$$

Thus, from equations 5.94 and 5.95, we get

$$A_1 = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.109}$$

$$b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{5.110}$$

$$c_1^T = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \tag{5.111}$$

And, from equations 5.107 and 5.108, we get

$$A_2 = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.112}$$

$$b_2 = \begin{bmatrix} \frac{1}{2L} \\ 0 \end{bmatrix} \tag{5.113}$$

$$c_2^T = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \tag{5.114}$$

Finally, from equations 5.9 and 5.10, we obtain the matrices

$$A = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \tag{5.115}$$

$$b = \begin{bmatrix} \frac{d+1}{2L} \\ 0 \end{bmatrix} \tag{5.116}$$

$$c^T = \begin{bmatrix} (R_c \,||R) & \frac{R}{R+R_c} \end{bmatrix} \tag{5.117}$$

Thus the dynamic equations for the center-point-clamped ac-ac converter system for region 2 are:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{d+1}{2L} \\ 0 \end{bmatrix} v_{in} \tag{5.118}$$

$$[v_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{5.119}$$

Now let us introduce a perturbation in input voltage (*u*) and duty ratio (*d*) causing a corresponding perturbation in state variables (*x*) and output (*y*).

$$x = X + \hat{x} \tag{5.120}$$

$$y = Y + \hat{y} \tag{5.121}$$

$$u = U + \hat{u} \tag{5.122}$$

$$d = D + \hat{d} \tag{5.123}$$

Substituting in equations 5.118 and 5.119,

$$\begin{bmatrix} \frac{dI_L}{dt} + \frac{d\widehat{\imath_L}}{dt} \\ \frac{dV_c}{dt} + \frac{d\widehat{v_C}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} I_L + \widehat{\imath_L} \\ V_c + \widehat{v_C} \end{bmatrix} + \begin{bmatrix} \frac{D+\hat{d}+1}{2L} \\ 0 \end{bmatrix} (V_{in} + \widehat{v_{in}}) \quad (5.124)$$

$$[V_o + \widehat{v_o}\,] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} I_L + \widehat{\imath_L} \\ V_c + \widehat{v_C} \end{bmatrix} \quad (5.125)$$

But, from equations 5.118 and 5.119,

$$\begin{bmatrix} \frac{dI_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{D+1}{2L} \\ 0 \end{bmatrix} V_{in} \quad (5.126)$$

$$[V_o] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} \quad (5.127)$$

Thus subtracting equation (5.126) from (5.124), and equation (5.127) from (5.125), we get

$$\begin{bmatrix} \frac{d\widehat{\imath_L}}{dt} \\ \frac{d\widehat{v_C}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_L+(R_c \,||R))}{L} & -\frac{R}{(R+R_c)L} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} \widehat{\imath_L} \\ \widehat{v_C} \end{bmatrix} + \begin{bmatrix} \frac{\hat{d}}{2L} \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} \frac{D+1}{2L} \\ 0 \end{bmatrix} \widehat{v_{in}} \quad (5.128)$$

$$[\widehat{v_o}\,] = \begin{bmatrix} R_c \,||\, R & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} \widehat{\imath_L} \\ \widehat{v_C} \end{bmatrix} \quad (5.129)$$

Transforming equation (5.128) to Laplace domain we get,

$$sL\widehat{\imath_L}(s) = -(R_L + R \,||\, R_C\,)\widehat{\imath_L}(s) - \frac{R}{(R+R_C)}\widehat{v_C}(s) + \frac{D+1}{2}\widehat{v_{in}}(s) + \frac{V_{in}}{2}\hat{d}(s)$$

(5.130)

$$sC\widehat{v_C}(s) = \frac{R}{R+R_C}\widehat{\imath_L}(s) - \frac{1}{R+R_C}\widehat{v_C}(s) \quad (5.131)$$

Rearranging,

$$(sC + \frac{1}{R+R_C})\widehat{v_C}(s) = \frac{R}{R+R_C}\widehat{\imath_L}(s) \quad (5.132)$$

$$(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{\imath_L}(s) \quad (5.133)$$

Similarly, transforming output equation (5.129) to Laplace domain we get

$$\widehat{v_o}(s) = (R \,||\, R_C\,)\widehat{\imath_L}(s) + \frac{R}{(R+R_C)}\widehat{v_C}(s) \quad (5.134)$$

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) - R_C\widehat{\imath_L}(s) = \widehat{v_C}(s) \quad (5.135)$$

Substituting from equation (5.133),

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) - R_C(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{v_C}(s) \quad (5.136)$$

$$\widehat{v_o}(s)\left(\frac{R+R_C}{R}\right) = R_C\left(sC\left(\frac{R+R_C}{R}\right) + \frac{1}{R}\right)\widehat{v_C}(s) + \widehat{v_C}(s) \quad (5.137)$$

$$\widehat{v_o}(s) = R_C\left(sC + \frac{1}{R+R_C}\right)\widehat{v_C}(s) + \left(\frac{R}{R+R_C}\right)\widehat{v_C}(s) \quad (5.138)$$

$$\widehat{v_o}(s) = sR_CC\,\widehat{v_C}(s) + \widehat{v_C}(s) \quad (5.139)$$

$$\widehat{v_o}(s) = (1 + sR_CC)\,\widehat{v_C}(s) \quad (5.140)$$

Substituting in equation (5.133),

$$(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_C}(s) = \widehat{\imath_L}(s) \quad (5.134)$$

$$\frac{1}{1+sR_CC}(sC(\frac{R+R_C}{R}) + \frac{1}{R})\,\widehat{v_o}(s) = \widehat{\imath_L}(s) \quad (5.135)$$

Substituting in equation (5.130),

$$sL\frac{1}{1+sR_CC}\left(sC\left(\frac{R+R_C}{R}\right)+\frac{1}{R}\right)\widehat{v_o}(s)=-(R_L+R\,||\,R_C)\frac{1}{1+sR_CC}\left(sC\left(\frac{R+R_C}{R}\right)+\frac{1}{R}\right)\widehat{v_o}(s)-\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)+\frac{D+1}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.136)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\widehat{v_o}(s)=-(R_L+R\,||\,R_C)\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\widehat{v_o}(s)-\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)+\frac{D+1}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.137)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\widehat{v_o}(s)+(R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{1+sR_CC}\frac{1}{R}\widehat{v_o}(s)+\frac{R}{(R+R_C)}\frac{1}{1+sR_CC}\widehat{v_o}(s)=\frac{D+1}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s) \quad (5.138)$$

$$sL\frac{1+sC(\mathrm{R+R_C})}{R}\widehat{v_o}(s)+(R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}\widehat{v_o}(s)+\frac{R}{(R+R_C)}\widehat{v_o}(s)=(1+sR_CC)\left(\frac{1+D}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)\right) \quad (5.139)$$

$$(sL+R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}\widehat{v_o}(s)+\frac{R}{(R+R_C)}\widehat{v_o}(s)=(1+sR_CC)\left(\frac{D+1}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)\right) \quad (5.140)$$

$$\left[(sL+R_L+R\,||R_C)\frac{1+sC(\mathrm{R+R_C})}{R}+\frac{R}{(R+R_C)}\right]\widehat{v_o}(s)=(1+sR_CC)\left(\frac{D+1}{2}\widehat{v_{in}}(s)+\frac{V_{in}}{2}\hat{d}(s)\right) \quad (5.141)$$

From equation (5.141), we get transfer functions as,

$$G_d=\left.\frac{\widehat{v_o}(s)}{\hat{d}(s)}\right|_{\widehat{v_{in}}(s)=0} \quad (5.142)$$

$$G_v=\left.\frac{\widehat{v_o}(s)}{\widehat{v_{in}}(s)}\right|_{\hat{d}(s)=0} \quad (5.143)$$

where G_d is the transfer function between the output voltage to duty ratio and G_v is the transfer function between the output voltage to input voltage.

Substituting equation (5.141) in (5.142) and (5.143), we obtain,

$$G_d = \frac{V_{in}}{2\left(\left[\frac{Cs\left(\frac{R+R_C}{R}\right)+\frac{1}{R}}{1+sCR_C}\right)(sL+R_L+R\,||R_C)\right]+\frac{R}{(R+R_C)}\right)} \tag{5.144}$$

$$G_v = \frac{D+1}{2\left(\left[\frac{Cs\left(\frac{R+R_C}{R}\right)+\frac{1}{R}}{1+sCR_C}\right)(sL+R_L+R\,||R_C)\right]+\frac{R}{(R+R_C)}\right)} \tag{5.145}$$

For desired output voltage ($v_{in}/2$ to v_{in}):

Transfer functions G_d and G_v are given by equations (5.144) and (5.145). Uncompensated bode plots of equation (5.144) and equation (5.145) are shown in figure 5.8 and figure 5.9.

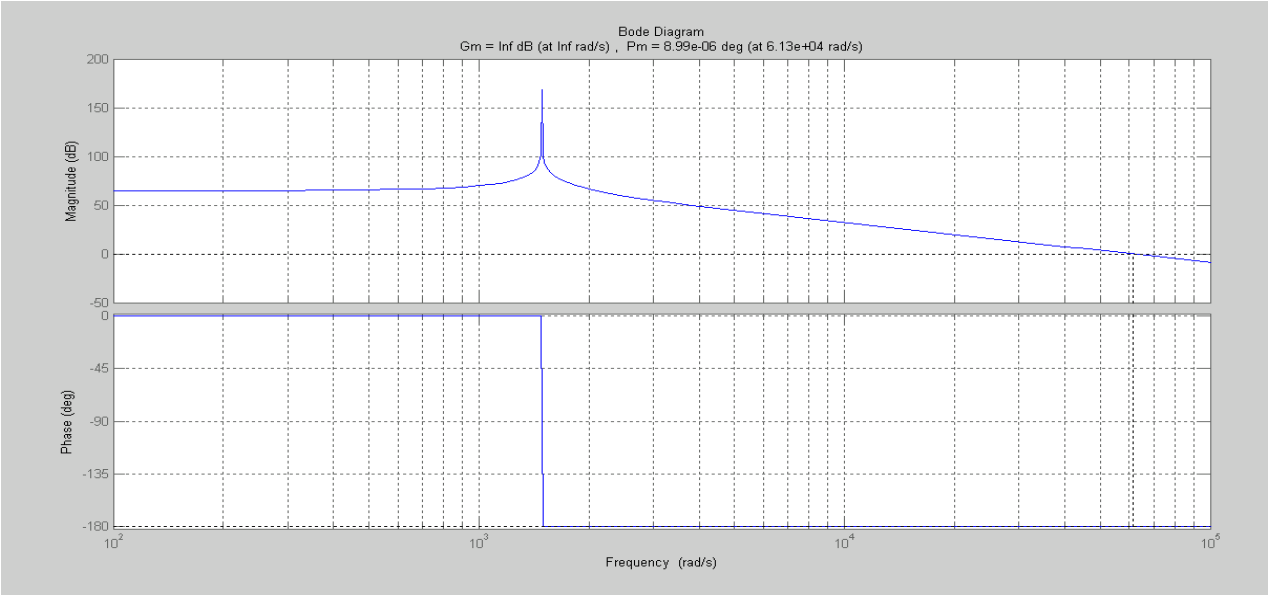


Figure 5.8: Magnitude and phase plots of transfer function G_d for output voltage range $v_{in}/2$ to v_{in}.

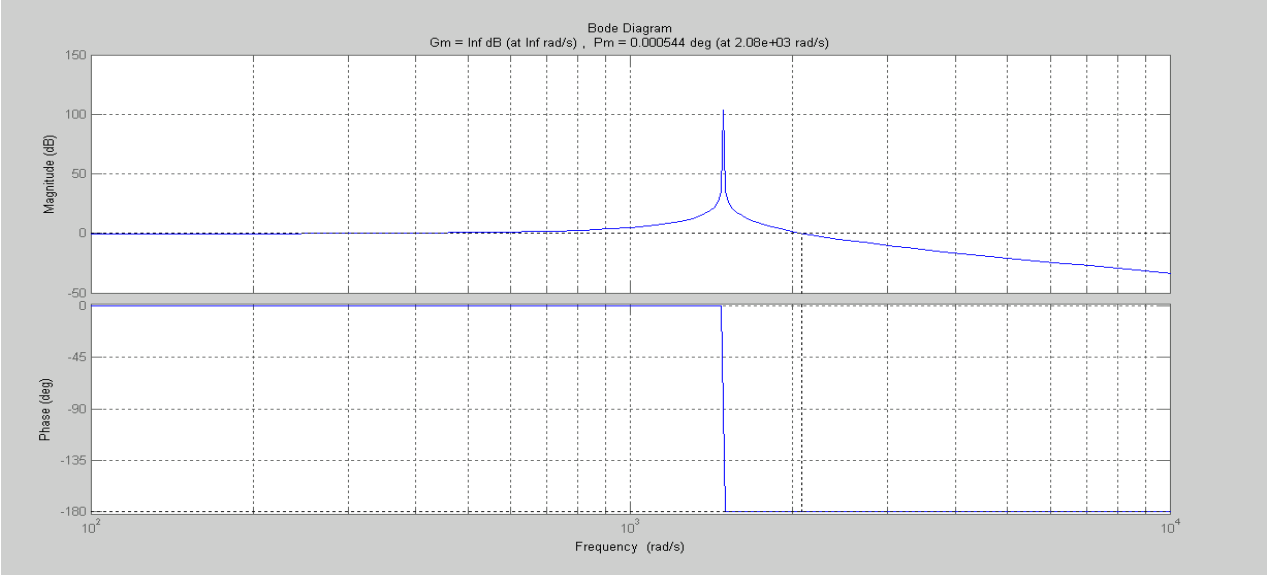


Figure 5.9: Magnitude and phase plots of transfer function G_v for output voltage range $v_{in}/2$ to v_{in}.

CHAPTER 6 : CONTROLLER DESIGN FOR CLOSED LOOP CONTROL OF CENTER-POINT-CLAMPED AC-AC CONVERTER

6.1. Introduction

The design of a feedback compensator for closed loop control of the center-point-clamped ac-ac buck converter has been discussed in this chapter. Transfer function G_d (transfer function between the output voltage to duty ratio) is used for designing the feedback compensator a MATLAB-SISO (Single Input/Single Output) tool. SISO tool is a GUI (Graphical User Interface) for compensator designs.

6.2. Circuit Description

A simplified circuit schematic of a single phase of center-point-clamped ac-ac buck converter is shown in figure 6.1.

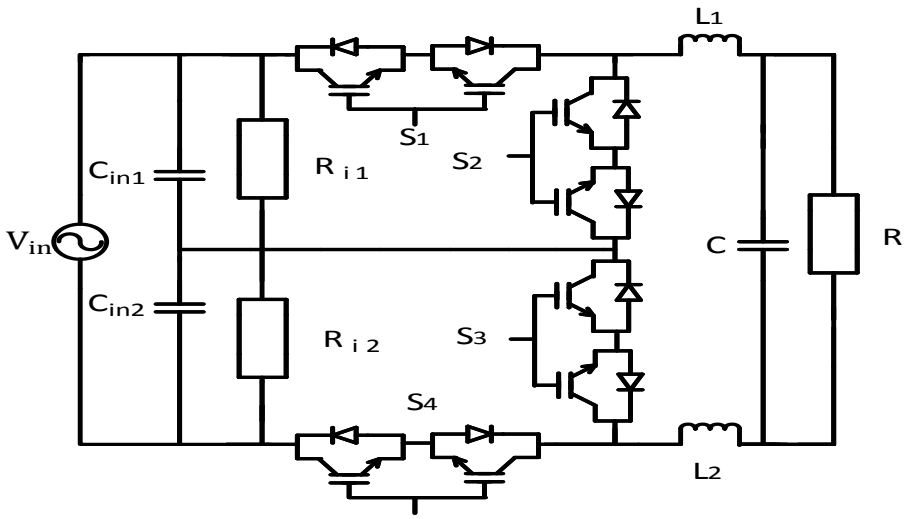


Figure 6.1: Simplified circuit schematic of a single phase of center-point-clamped ac-ac buck converter.

A representative center-point-clamped ac-ac converter circuit description is same as given in chapter 4.

6.3. Compensator Design

Using the transfer function G_d (transfer function between the output voltage to duty ratio), a feedback compensator has been designed to make the center point clamped ac-ac converter stable. MATLAB SISO tool has been used to design the feedback compensator for the converter. As may be seen from the Bode plots of the transfer function of the uncompensated converter system, the gain margin is infinity, but the phase margin is very little. In order to make the converter stable for all regions of operation, the phase margin has to be improved to at least fifty degrees. It may also be seen from the unit step input response of the uncompensated converter system that the peak amplitude rises to about 200 percent of unity, thus making the converter system underdamped. SISO tool gets updated G_d, from MATLAB workspace and produces closed loop and open loop bode plots. To improve the phase and gain margin of the bode plot, pole should either be placed/moved to the right and the zero towards left of the bode plot.

The compensator G_c is given by,

$$G_c = \frac{(1 + 0.023s)}{s\,(1 + 0.0001\,s)} \tag{6.1}$$

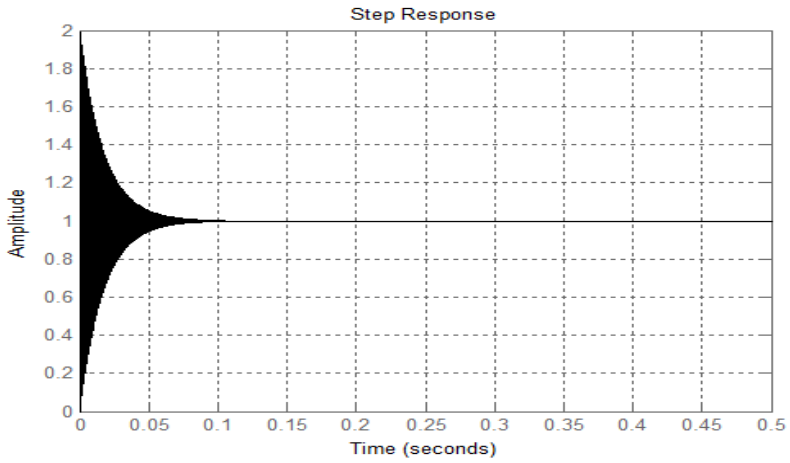


Figure 6.2: Step response plot of uncompensated converter output voltage to duty cycle transfer function, G_d.

For the uncompensated transfer function G_d, the designed feedback compensator (G_c) has damped the peak overshoot, good command following performance as the system exhibits good line regulation and fast transient response. This compensator G_c is employed in the converter system as shown in figure 6.3.

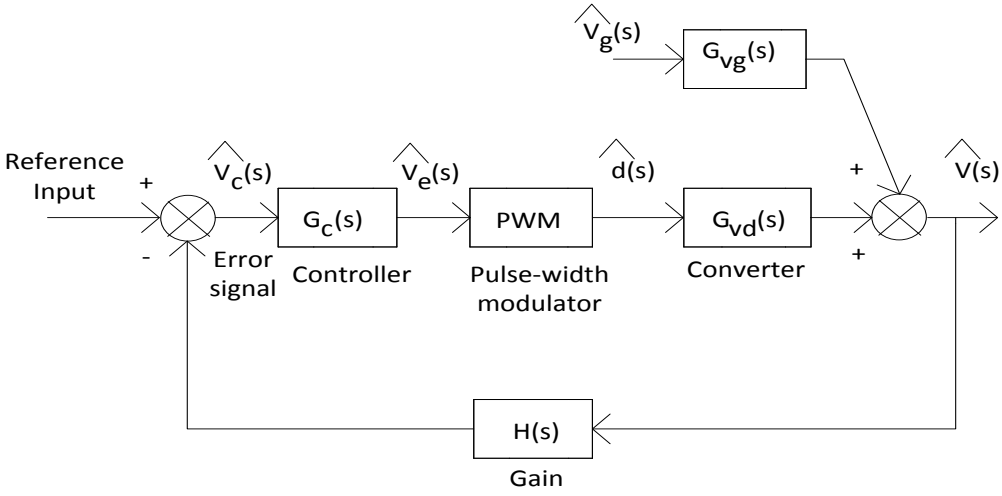


Figure 6.3: Control block diagram of center-point-clamped ac-ac converter.

It may be seen from figure 6.4 that the addition of the feedback controller has improved the phase margin to 50 degrees. Also, it may be observed from figure 6.5 that the unit

step input response of the transfer function, G_d*G_c of the compensated converter system that the system peak overshoot has been damped.

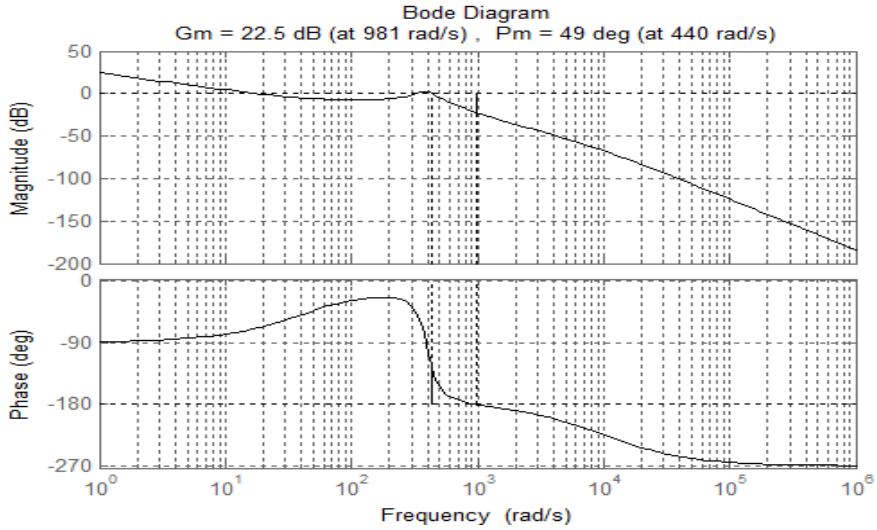


Figure 6.4: Magnitude and phase plots of transfer function G_d*G_c for output voltage range 0 to v_{in}.

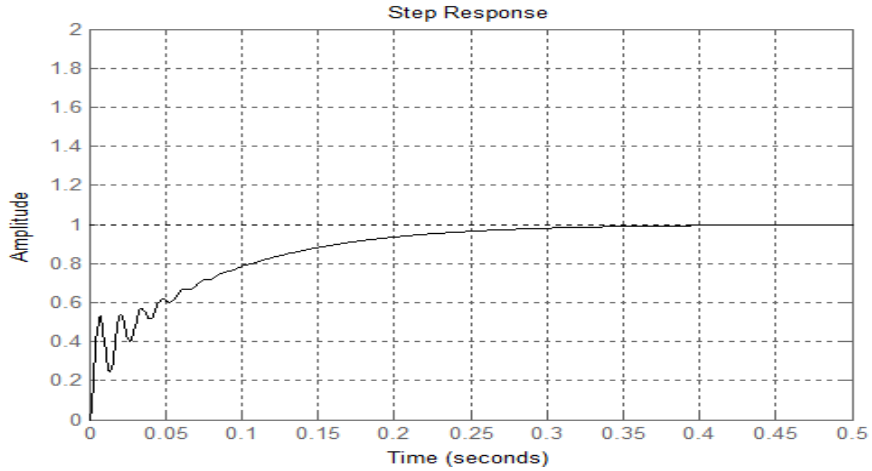


Figure 6.5: Step response plot of transfer function G_d*G_c for output voltage range 0 to v_{in}.

CHAPTER 7 : INPUT FILTER CONSIDERATIONS FOR CENTER-POINT-CLAMPED AC-AC CONVERTER

7.1. Introduction

The design of input filter for power converters in critical applications must adhere to the EMI (Electro-Magnetic Interference) norms for various application domains, such as defense, aerospace and telecommunication industry [28], [29]. It may be seen that an input filter may be designed that closely conforms to the harmonic and EMI standards, but it might cause significant performance degradation of the power converter itself. The performance degradation is attributed to the introduction of additional states in the system, which leads to change in the converter transfer functions as well as change in converter source impedance [30]. Thus, it may be seen that although input filter is necessary to reject harmonics in the input current due to switching in the converter as well as to protect converter from input voltage transients, yet care must be taken in designing the input filter and the corresponding controller such that it does not alter the converter performance or destabilize the converter [31]-[36]. This chapter deals with the input filter design considerations for a Center-Point-Clamped AC-AC converter. It may be seen in the following sections that the designed input filter improves the spectral performance of the converter. A feedback controller is designed which significantly improves the phase margin of the converter system.

7.2. Modified Center-Point-Clamped AC-AC Converter Circuit

Modified circuit schematic of a single phase Center-Point-Clamped AC-AC converter with the introduction of an input side inductor, L_i is shown in figure 7.1.

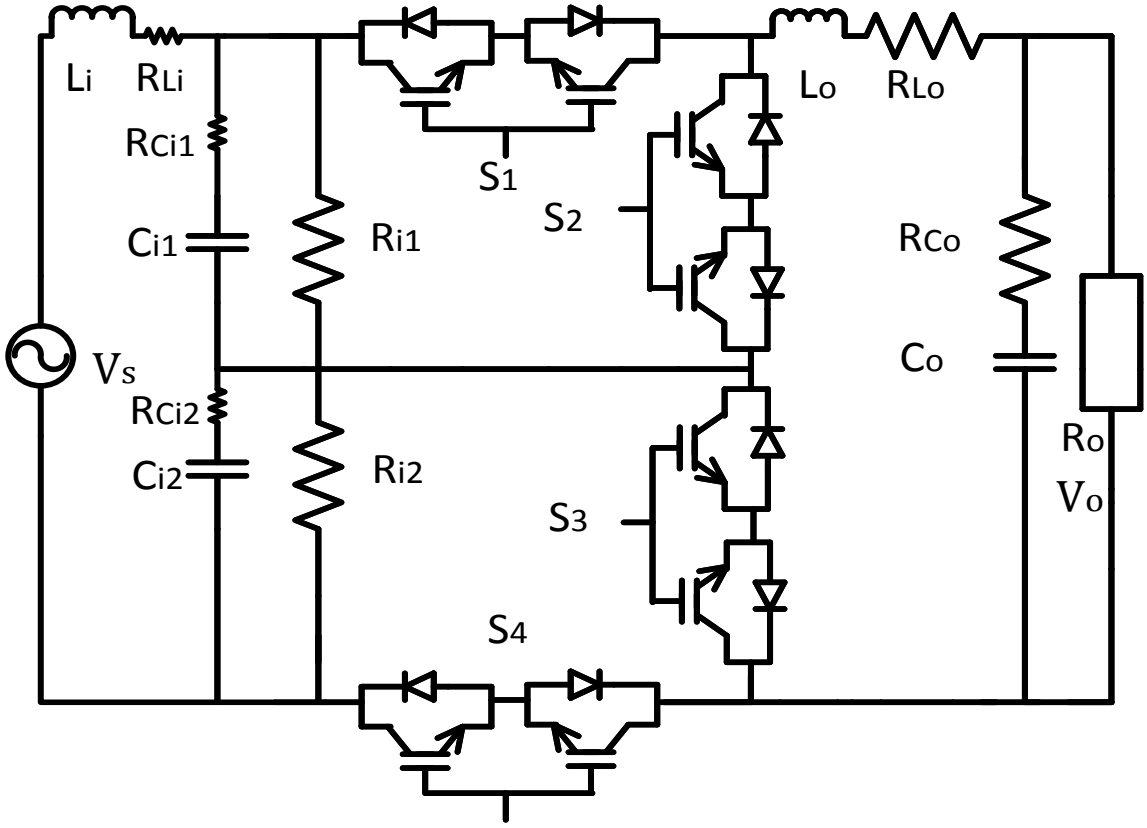


Figure 7.1: Simplified circuit schematic of Center-Point-Clamped AC-AC converter with input filter.

It may be seen from [31] that a switched mode converter due to its switching action feeds in discontinuous current from its input side. It may be observed that this discontinuous current contains harmonics which may be expressed as a function of the switching function. These harmonics are in the order of multiples of switching frequency. Thus, they may be filtered out using a low pass filter. As may be seen from figure 7.1, an inductor has been introduced into the modified center-point-clamped ac-ac buck converter circuit schematic to form a low pass filter with the input side capacitors, C_{i1}

and C_{i2}. This filter removes the unwanted harmonic currents fed into the unregulated input power supply. But the introduction of the input filter has destabilizing effect on the converter as the source impedance gets changed. The effect in the performance and stability of the converter due to input filter is studied in the following sections.

7.3. Description of Modified Center-Point-Clamped AC-AC Buck Converter Circuit

As may be seen from figure 7.1, V_s is the input voltage source, L_i is the input side inductor and R_{Li} is the parasitic resistance involved with L_i, C_{i1} and C_{i2} are the input side voltage balancing capacitors, R_{Ci1} and R_{Ci2} are the parasitic resistances involved with C_{i1} and C_{i2}, R_{i1} and R_{i2} are the input side resistances behaving as a potential divider, S_1, S_2, S_3 and S_4 are the four bidirectional switches realized by IGBTs, L_o is the output side inductor and R_{Lo} is the parasitic resistance associated with it, C_o is the output side capacitor and R_{Co} is the parasitic resistance of C_o, and V_o is the voltage across the load resistor, R_o.

7.4. Dynamic Analysis of Modified Center-Point-Clamped AC-AC Buck Converter

It may be observed that the introduction of an inductor to form the input side low pass filter would change the converter transfer functions obtained in Section 5.4. It is so because the addition of the input filter introduces new states into the converter state space equations obtained in Section 5.3. Also, it may be seen from figure.7.1 that the modified converter circuit schematic incorporates the parasitic resistances involved with the components, L_i, C_{i1}, C_{i2}, L_o, and C_o. A new dynamic analysis of the modified converter circuit, as shown has been performed using state space averaging technique. Here, the dynamics involved with the input side inductor and capacitors have been taken into account. Thus, the assumption that input voltage is split evenly between the two filter

capacitors at any given time has been ignored in this analysis, rather the dynamics associated with the capacitor voltages have also been examined in the analysis. It has been assumed that the converter is operating in continuous conduction mode. As already discussed in Section 5.4, the converter has two regions, in region 1 desired output voltage ranges from 0 to $v_s/2$, and in region 2 desired output voltage ranges from $v_s/2$ to v_s. Here, the state variables are input filter inductor current, i_s, input filter capacitor voltages, v_{Ci1} and v_{Ci2}, output filter inductor current, i_{Lo}, and output filter capacitor voltage, v_{Co}. The dynamic analysis is performed for both regions as shown in Section 5.4 and the state space equations derived for both the regions of converter operation are shown as follows:

Region1: (Reference voltage ranges between 0 to $v_s/2$)

$$\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dv_{Ci1}}{dt} \\ \frac{dv_{Ci2}}{dt} \\ \frac{di_{Lo}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} = A_1 * \begin{bmatrix} i_s \\ v_{Ci1} \\ v_{Ci2} \\ i_{Lo} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{7.1}$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} i_s \\ v_{Ci1} \\ v_{Ci2} \\ i_{Lo} \\ v_{Co} \end{bmatrix} \tag{7.2}$$

where, A_1 is

$$\begin{bmatrix} -R_{Li} - \frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} - \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})} & -\frac{(R_{i1})}{(R_{Ci1}+R_{i1})} & -\frac{(R_{i2})}{(R_{Ci2}+R_{i2})} & \left(d * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ \frac{(R_{i1})}{(R_{Ci1}+R_{i1})} & -\frac{(1)}{(R_{Ci1}+R_{i1})} & 0 & \frac{(d*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ \frac{(R_{i2})}{(R_{Ci2}+R_{i2})} & 0 & -\frac{(1)}{(R_{Ci2}+R_{i2})} & \frac{(d*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(d * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(d*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(d*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -R_{Lo} - \left(d * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) - \frac{(R_{Co}*R_o)}{(R_{Co}+R_o)} & -\frac{(R_{Co}*R_o)}{(R_{Co}+R_o)} \\ 0 & 0 & 0 & \frac{(R_o)}{(R_{Co}+R_o)} & -\frac{(1)}{(R_{Co}+R_o)} \end{bmatrix}$$

Region2: (Reference voltage ranges between $v_s/2$ to v_s):

$$\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dv_{Ci1}}{dt} \\ \frac{dv_{Ci2}}{dt} \\ \frac{di_{Lo}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} = A_2 * \begin{bmatrix} i_s \\ v_{Ci1} \\ v_{Ci2} \\ i_{Lo} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{7.3}$$

$$v_o = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} i_s \\ v_{Ci1} \\ v_{Ci2} \\ i_{Lo} \\ v_{Co} \end{bmatrix} \tag{7.4}$$

A_2 is

$$\begin{bmatrix} -R_{Li} - \frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} - \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})} & -\frac{(R_{i1})}{(R_{Ci1} + R_{i1})} & -\frac{(R_{i2})}{(R_{Ci2} + R_{i2})} & \left((1-d) * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2} \right) & 0 \\ \frac{(R_{i1})}{(R_{Ci1} + R_{i1})} & -\frac{(1)}{(R_{Ci1} + R_{i1})} & 0 & \frac{((1-d) * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & 0 \\ \frac{(R_{i2})}{(R_{Ci2} + R_{i2})} & 0 & -\frac{(1)}{(R_{Ci2} + R_{i2})} & \frac{((1-d) * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 \\ \left((1-d) * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2} \right) & \frac{((1-d) * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & \frac{((1-d) * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & -R_{Lo} - \left((1-d) * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2} \right) - \frac{(R_{Co} * R_o)}{(R_{Co} + R_o)} & -\frac{(R_{Co} * R_o)}{(R_{Co} + R_o)} \\ 0 & 0 & 0 & \frac{(R_o)}{(R_{Co} + R_o)} & -\frac{(1)}{(R_{Co} + R_o)} \end{bmatrix}$$

Introducing a perturbation in input voltage, v_s, input side inductor current, i_s, input side capacitor voltages, v_{Ci1} and v_{Ci2} , duty ratio d, output side inductor current, i_{Lo} and output side capacitor voltage, v_{Co} causes a corresponding perturbation in state variables i_s, v_{Ci1}, v_{Ci2}, i_{Lo}, and v_{Co}, and output v_o, as follows:

$$v_s = V_s + \widehat{v_s} \tag{7.5}$$

$$i_s = I_s + \widehat{i_s} \tag{7.6}$$

$$v_{Ci1} = V_{Ci1} + \widehat{v_{Ci1}} \tag{7.7}$$

$$v_{Ci2} = V_{Ci2} + \widehat{v_{Ci2}} \tag{7.8}$$

$$d = D + \hat{d} \tag{7.9}$$

$$i_{Lo} = I_{Lo} + \widehat{i_{Lo}} \tag{7.10}$$

$$v_{Co} = V_{Co} + \widehat{v_{Co}} \tag{7.11}$$

$$v_o = V_o + \widehat{v_o} \tag{7.12}$$

where the capitalized variables represent the steady state values and the variables in hat (^) representation are the small perturbations introduced in steady state parameters. Approximating that perturbations are negligible as compared to the steady state values, small signal state space equations for center-point-clamped ac-ac converter circuit are

Region1: (Reference voltage ranges between 0 to v_s/2)

$$\begin{bmatrix} \frac{d(I_s+\widehat{i_s})}{dt} \\ \frac{d(V_{Ci1}+\widehat{v_{Ci1}})}{dt} \\ \frac{d(V_{Ci2}+\widehat{v_{Ci2}})}{dt} \\ \frac{d(I_{Lo}+\widehat{i_{Lo}})}{dt} \\ \frac{d(V_{Co}+\widehat{v_{Co}})}{dt} \end{bmatrix} = \left(A_1 + \widehat{A_1}\right) * \begin{bmatrix} I_s + \widehat{i_s} \\ V_{Ci1} + \widehat{v_{Ci1}} \\ V_{Ci2} + \widehat{v_{Ci2}} \\ I_{Lo} + \widehat{i_{Lo}} \\ V_{Co} + \widehat{v_{Co}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (V_s + \widehat{v_s}) \tag{7.13}$$

$$(V_o + \widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} I_s + \widehat{i_s} \\ V_{Ci1} + \widehat{v_{Ci1}} \\ V_{Ci2} + \widehat{v_{Ci2}} \\ I_{Lo} + \widehat{i_{Lo}} \\ V_{Co} + \widehat{v_{Co}} \end{bmatrix} \tag{7.14}$$

where $\widehat{A_1}$ is

$$\begin{bmatrix} 0 & 0 & 0 & \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 \\ \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 & 0 \\ 0 & 0 & 0 & -\left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ & & & 0 & \end{bmatrix}$$

Region2: (Reference voltage ranges between $v_s/2$ to v_s)

$$\begin{bmatrix} \frac{d(I_s+\widehat{\imath_s})}{dt} \\ \frac{d(V_{Ci1}+\widehat{v_{Ci1}})}{dt} \\ \frac{d(V_{Ci2}+\widehat{v_{Ci2}})}{dt} \\ \frac{d(I_{Lo}+\widehat{\imath_{Lo}})}{dt} \\ \frac{d(V_{Co}+\widehat{v_{Co}})}{dt} \end{bmatrix} = \left(A_2 + \widehat{A_2}\right) * \begin{bmatrix} I_s + \widehat{\imath_s} \\ V_{Ci1} + \widehat{v_{Ci1}} \\ V_{Ci2} + \widehat{v_{Ci2}} \\ I_{Lo} + \widehat{\imath_{Lo}} \\ V_{Co} + \widehat{v_{Co}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (V_s + \widehat{v_s}) \tag{7.15}$$

$$(V_o + \widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} I_s + \widehat{\imath_s} \\ V_{Ci1} + \widehat{v_{Ci1}} \\ V_{Ci2} + \widehat{v_{Ci2}} \\ I_{Lo} + \widehat{\imath_{Lo}} \\ V_{Co} + \widehat{v_{Co}} \end{bmatrix} \tag{7.16}$$

where $\widehat{A_2}$ is

$$\begin{bmatrix} 0 & 0 & 0 & \left(\hat{d} * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d}*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d}*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(\hat{d} * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(\hat{d}*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(\hat{d}*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -\left(\hat{d} * \frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

Upon elimination of the steady state terms from equations, (7.13), (7.14), (7.15) and (7.16) and neglecting the second order differential terms as they are assumed to be very negligible, the new set of state space equations are

Region1: (Reference voltage ranges between 0 to $v_s/2$)

$$\begin{bmatrix} \frac{d(\widehat{\imath_s})}{dt} \\ \frac{d(\widehat{v_{Ci1}})}{dt} \\ \frac{d(\widehat{v_{Ci2}})}{dt} \\ \frac{d(\widehat{\imath_{Lo}})}{dt} \\ \frac{d(\widehat{v_{Co}})}{dt} \end{bmatrix} = (A_1) * \begin{bmatrix} \widehat{\imath_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{\imath_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} + \left(\widehat{A_1}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \tag{7.17}$$

$$(\widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} \tag{7.18}$$

where $\widehat{A_1}$ is

$$\begin{bmatrix} 0 & 0 & 0 & \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2}+R_{i2}))} & 0 \\ \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1}+R_{i1}))} & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2}+R_{i2}))} & -\left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1}+R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

<u>Region2: (Reference voltage ranges between v_s/2 to v_s)</u>

$$\begin{bmatrix} \frac{d(\widehat{i_s})}{dt} \\ \frac{d(\widehat{v_{Ci1}})}{dt} \\ \frac{d(\widehat{v_{Ci2}})}{dt} \\ \frac{d(\widehat{i_{Lo}})}{dt} \\ \frac{d(\widehat{v_{Co}})}{dt} \end{bmatrix} = (A_2) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} + (\widehat{A_2}) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \tag{7.19}$$

$$(\widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} \tag{7.20}$$

where $\widehat{A_2}$ is

$$\begin{bmatrix} 0 & 0 & 0 & \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 \\ \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & -\left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

Now, transforming the above time domain equations, (7-17), (7-18), (7-19) and (7-20) into Laplace domain, we have,

<u>Region1: (Reference voltage ranges between 0 to v_s/2)</u>

$$sI * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (A_1) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} + \left(\widehat{A_1}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } (sI - A_1) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = \left(\widehat{A_1}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } (sI - A_1)^{-1} * (sI - A_1) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_1)^{-1} * \left(\widehat{A_1}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix}$$

$$+ (sI - A_1)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_1)^{-1} * \left(\widehat{A_1}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + (sI - A_1)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \qquad (7.21)$$

Also,

$$\widehat{A_1}=\begin{bmatrix} 0 & 0 & 0 & \left(\hat{d}*\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d}*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d}*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(\hat{d}*\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(\hat{d}*R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(\hat{d}*R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -\left(\hat{d}*\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

$$\text{or, } \widehat{A_1} = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -\left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix} * \hat{d}$$

$$\text{or, } \widehat{A_1} = A_1{}' * \hat{d} \tag{7.22}$$

where,

$$A_1{}' = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -\left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

Using the equation (7-22) in equation (7-21), we have,

$$\begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_1)^{-1} * \left(A_1{}'\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} * \left(\hat{d}\right) + (sI - A_1)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \tag{7.23}$$

From equation (7-18), we have,

$$(\widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} \quad (7.24)$$

Now, equating (6-23) and (6-24), we have,

$$(\widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} * (sI - A_1)^{-1} * \left(A_1{}'\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} * (\hat{d}) +$$

$$\begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} * (sI - A_1)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \quad (7.25)$$

From equation (7-25), the converter output voltage ($\widehat{v_o}$) to duty ratio transfer function ($\hat{d}$), G_{d1} may be found as follows

$$G_{d1} = \frac{\widehat{v_o}(s)}{\hat{d}(s)}_{\widehat{v_{in}}(s)=0} \quad \text{.....(7-26)}$$

$$\text{or, } G_{d1} = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} * (sI - A_1)^{-1} * \left(A_1{}'\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} \quad (7\text{-}27)$$

<u>Region2: (Reference voltage ranges between v_s/2 to v_s)</u>

On performing Laplace transformation of equation (6-19), we have

$$sI * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (A_2) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} + \left(\widehat{A_2}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } (sI - A_2) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = \left(\widehat{A_2}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } (sI - A_2)^{-1} * (sI - A_2) * \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_2)^{-1} * \left(\widehat{A_2}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix}$$

$$+ (sI - A_2)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s})$$

$$\text{or, } \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_2)^{-1} * \left(\widehat{A_2}\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} + (sI - A_2)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \quad (7.26)$$

Also,

$$\widehat{A_2} = \begin{bmatrix} 0 & 0 & 0 & \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 \\ \left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & \frac{(\hat{d} * R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & \frac{(\hat{d} * R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & -\left(\hat{d} * \frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

$$\text{or, } \widehat{A_2} = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & 0 \\ \left(\frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & \frac{(R_{i1})}{(2 * (R_{Ci1} + R_{i1}))} & \frac{(R_{i2})}{(2 * (R_{Ci2} + R_{i2}))} & -\left(\frac{\left(\frac{(R_{Ci1} * R_{i1})}{(R_{Ci1} + R_{i1})} + \frac{(R_{Ci2} * R_{i2})}{(R_{Ci2} + R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix} * \hat{d}$$

$$\text{or, } \widehat{A_2} = A_2{}' * \hat{d} \quad (7.27)$$

where,

$$A_2{}' = \begin{bmatrix} 0 & 0 & 0 & \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & 0 \\ 0 & 0 & 0 & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & 0 \\ \left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & \frac{(R_{i1})}{(2*(R_{Ci1}+R_{i1}))} & \frac{(R_{i2})}{(2*(R_{Ci2}+R_{i2}))} & -\left(\frac{\left(\frac{(R_{Ci1}*R_{i1})}{(R_{Ci1}+R_{i1})}+\frac{(R_{Ci2}*R_{i2})}{(R_{Ci2}+R_{i2})}\right)}{2}\right) & 0 \\ 0 & 0 & 0 & 0 & \end{bmatrix}$$

Using the equation (7-27) in equation (6-26), we have,

$$\begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} = (sI - A_2)^{-1} * \left(A_2{}'\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} * \left(\hat{d}\right) + (sI - A_2)^{-1} * \begin{bmatrix} \frac{1}{L_i} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} (\widehat{v_s}) \tag{7.28}$$

From equation (7-20), we have,

$$(\widehat{v_o}) = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} \begin{bmatrix} \widehat{i_s} \\ \widehat{v_{Ci1}} \\ \widehat{v_{Ci2}} \\ \widehat{i_{Lo}} \\ \widehat{v_{Co}} \end{bmatrix} \tag{7.29}$$

From equation (7.25), the converter output voltage ($\widehat{v_o}$) to duty ratio transfer function ($\hat{d}$), G_{d2} may be found as follows

$$G_{d2} = \frac{\widehat{v_o}(s)}{\hat{d}(s)}_{\widehat{v_{in}}(s)=0} \tag{7.26}$$

$$\text{or, } G_{d2} = \begin{bmatrix} 0 & 0 & 0 & \frac{R_{Co}*R_o}{R_{Co}+R_o} & \frac{R_o}{R_{Co}+R_o} \end{bmatrix} * (sI - A_2)^{-1} * \left(A_2{}'\right) * \begin{bmatrix} I_s \\ V_{Ci1} \\ V_{Ci2} \\ I_{Lo} \\ V_{Co} \end{bmatrix} \tag{7-27}$$

7.5. Input Filter Considerations for Center-Point-Clamped AC-AC Converter Circuit

The effect in the performance and stability of the converter due to input filter is studied in this section. It may be seen from the converter system dynamic analysis performed in Chapter 5, the dynamics pertaining to L_i, C_{i1}, and C_{i2} has been neglected for simplicity of analysis.

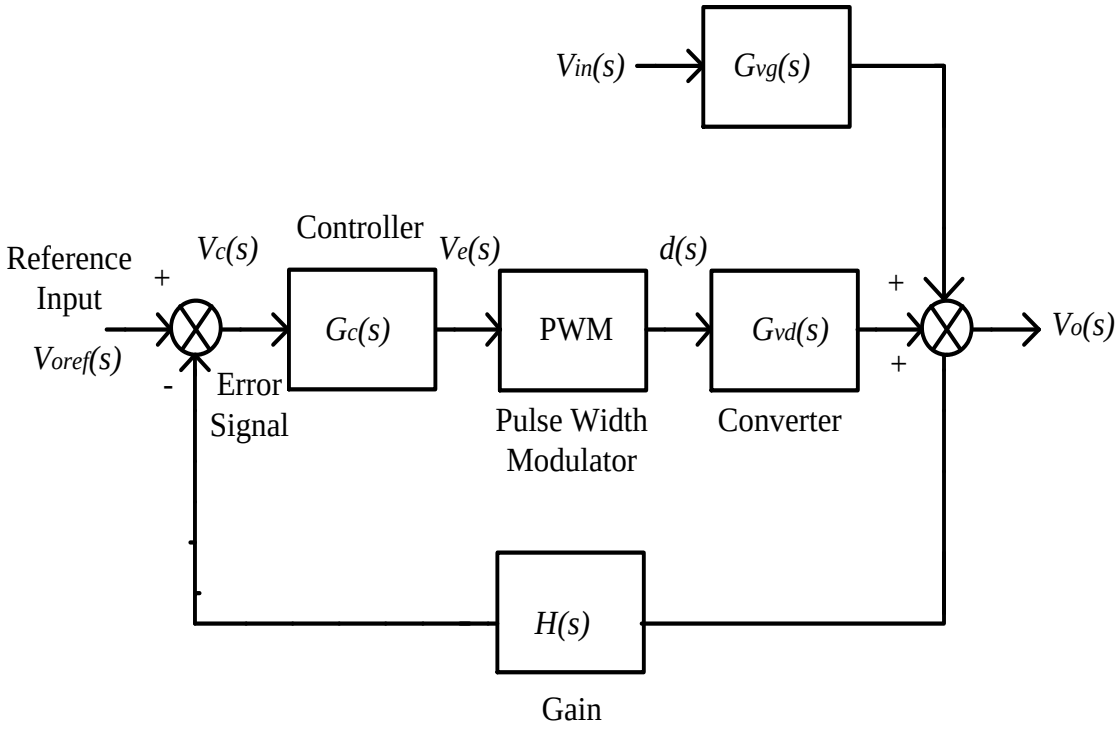


Figure 7.2: Simplified circuit schematic of Center-Point-Clamped AC-AC converter with input filter.

It has been assumed that the input voltage is split evenly between the two input side filter capacitors, i.e center-point at any given time [37]. But the input filter plays an important role in filtering out the unwanted harmonic currents fed into the unregulated input power supply [31]-[36] as well as to clamp the midpoint voltage level. Also, it may be seen from [30], [31], [39], that a switched mode converter due to its switching action feeds in

discontinuous current from its input side. It may be observed that this discontinuous current contains harmonics which may be expressed as a function of switching frequency. These harmonics are in the order of multiples of switching frequency. Thus, they may be filtered out using a low pass filter. As may be seen from figure 7.1, an inductor is present in input side of the center-point-clamped ac-ac buck converter circuit schematic to form a low pass filter with input side capacitors, C_{i1} and C_{i2}. This filter removes unwanted harmonic currents fed into the unregulated input power supply. But the introduction of input filter may have a destabilizing effect on the converter as source impedance gets changed. In order to analyze the effect of input side filter in performance and stability of the converter, state variables pertaining to input side filter components, voltage across L_i, current through capacitors, C_{i1} and C_{i2}, have to be taken into account while deriving dynamic equations of converter using state space averaging technique. It may be observed that the state space equation then would involve a state space matrix of 5x5 dimensions. Hence, it may be noted that it would be really difficult to derive converter transfer functions after the introduction of perturbation in five state variables involved in the dynamic equations.

This section discusses a technique to simplify the algebra involved in deriving the converter transfer functions, which incorporates the dynamics associated with all the possible state variables viz. five state variables for the system shown in figure 7.1. It may be seen in [38], that the dynamics of input filter may be incorporated in the transfer function G_{vd} (converter duty ratio to output voltage transfer function without introducing input filter) by using Middlebrook's extra element theorem. According to the theorem, the input filter is considered as an extra element having impedance $Z_o(s)$ and the

modified $G_{vd}(s)$, may be written as in eqn. (2). The converter system with the addition of an input filter is illustrated as a block diagram in figure. 7-3. The above equation implies that addition of an input filter modifies $G_{vd}(s)$ by a factor of $\frac{\left(1+\frac{Z_o(s)}{Z_N(s)}\right)}{\left(1+\frac{Z_o(s)}{Z_D(s)}\right)}$. Here, $Z_N(s)$ and $Z_D(s)$ are numerator and denominator of the input impedance, $Z_i(s)$ as seen from the converter with the addition of the input L-C filter comprising of L_i, C_{i1} and C_{i2}.

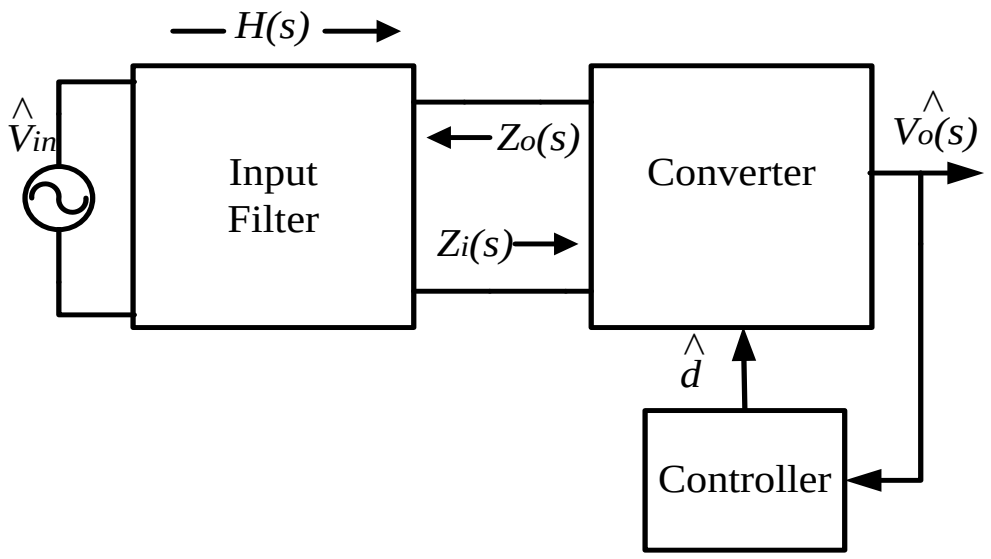


Figure 7.3: Generalized block schematic of a converter with an input filter in addition to the output filter

$$G_{vd}^{/}(s) = \left(G_{vd}(s)\right)\frac{\left(1+\frac{Z_o(s)}{Z_N(s)}\right)}{\left(1+\frac{Z_o(s)}{Z_D(s)}\right)} \tag{7.28}$$

$$\|Z_o(s)\| \ll \|Z_N(s)\| \tag{7.29}$$

$$\|Z_o(s)\| \ll \|Z_D(s)\| \tag{7.30}$$

$$G_{vd}(s) = \frac{9.35*10^{-05}\,s + 3400}{4.1*10^{-07}\,s^2 + 0.001439\,s + 2} \tag{7.31}$$

$$Z_o(s) = \frac{1.62*10^{-25}\,s^5 + 1.62*10^{-18}\,s^4 + 1.782*10^{-16}\,s^3 + 1.674*10^{-15}\,s^2 + 5.46*10^{-15}\,s^1 + 6*10^{-15}}{8.1*10^{-23}\,s^5 + 1.08*10^{-20}\,s^4 + 1.62*10^{-14}\,s^3 + 1.62*10^{-13}\,s^2 + 5.4*10^{-13}\,s^1 + 6*10^{-13}} \quad (7.32)$$

$$Z_N(s) = 1003 \quad (7.33)$$

$$Z_D(s) = \frac{5.843*10^{-11}\,s^3 + 2.05*10^{-07}\,s^2 + 0.000285\,s}{2.85*10^{-09}\,s^2 + 1*10^{-05}\,s} \quad (7.34)$$

It is also stated in [30], [31], [39], that even with addition of input filter, converter would retain its original dynamics if inequalities (7.29) and (7.30) are satisfied. It implies, when the input filter is designed such that considerations (7.29) and (7.30) are met, the introduction of state variables associated with the input filter in dynamic equations would have no effect in the behavior of the dynamic equations obtained in Table 2. Thus, it may be seen from eqns. (7.28), (7.29) and (7.30) that if the inequalities in eqn. (7.29) and (7.30) are strictly followed while designing the input filter, the new converter duty ratio to output voltage transfer function, $G_{vd}^{/}(s)$, would be same as original transfer function, $G_{vd}\,(s)$, since the factor of $\frac{\left(1+\frac{Z_o(s)}{Z_N(s)}\right)}{\left(1+\frac{Z_o(s)}{Z_D(s)}\right)}$ that is introduced due to addition of input filter [38] would approximately become unity. Hence, it may be concluded from above discussions that these inequalities (7.29) and (7.30) serve as necessary design considerations for selection of parameters of input filter of center-point-clamped ac-ac buck converter. The values of designed input filter parameters along with the other converter parameters are

tabulated in Table 3 in the following chapter. The converter transfer functions derived with the parameters in Table 3 are shown in above equations (7.30)-(7.33). The Bode plots of transfer functions, $Z_o(s)$, $Z_N(s)$, and $Z_D(s)$ are shown in figure 7.4. It may be seen from the Bode magnitude plots in figure 7.4 that the input filter parameters in Table 3 are designed such that the inequalities are satisfied. This implies from our argument that the Bode magnitude and phase plots for $G_{vd}(s)$ and $G_{vd}^{/}(s)$ should be identical.

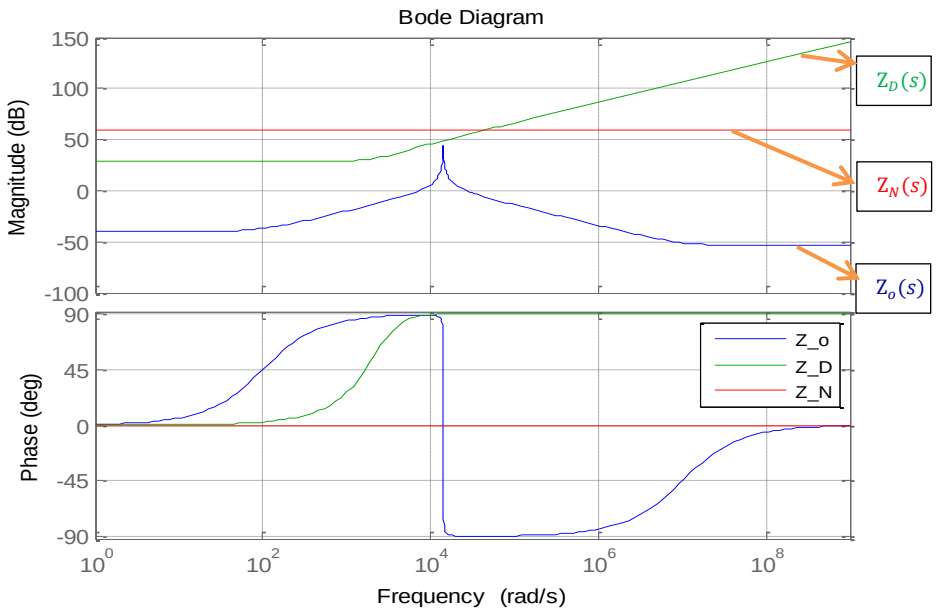


Figure 7.4: Bode plots for $Z_o(s)$, $Z_N(s)$ and $Z_D(s)$

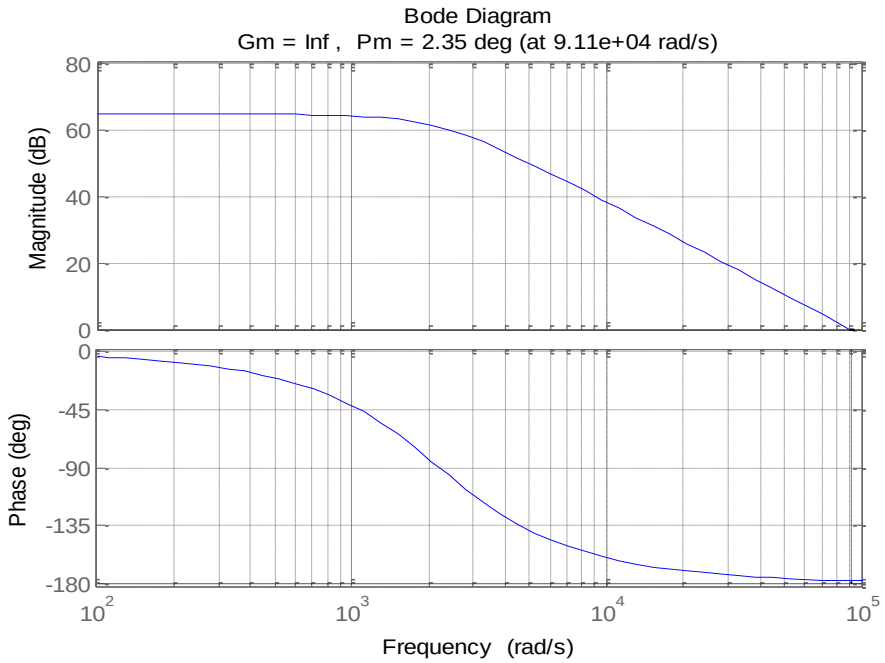


Figure 7.5: Bode plot for $G_{vd}\,(s)$

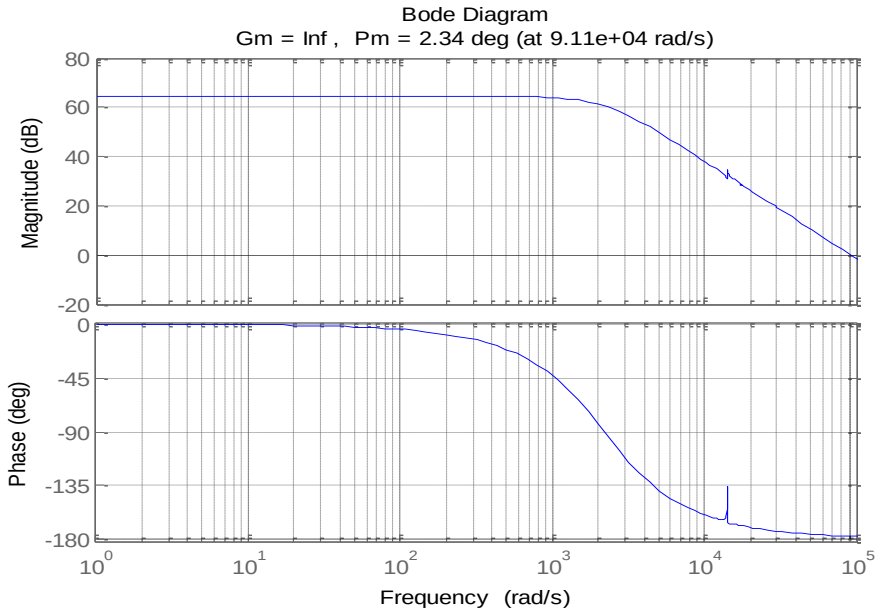


Figure 7.6: Bode plot of uncompensated transfer function, $G_{vd}^{/}$(s)

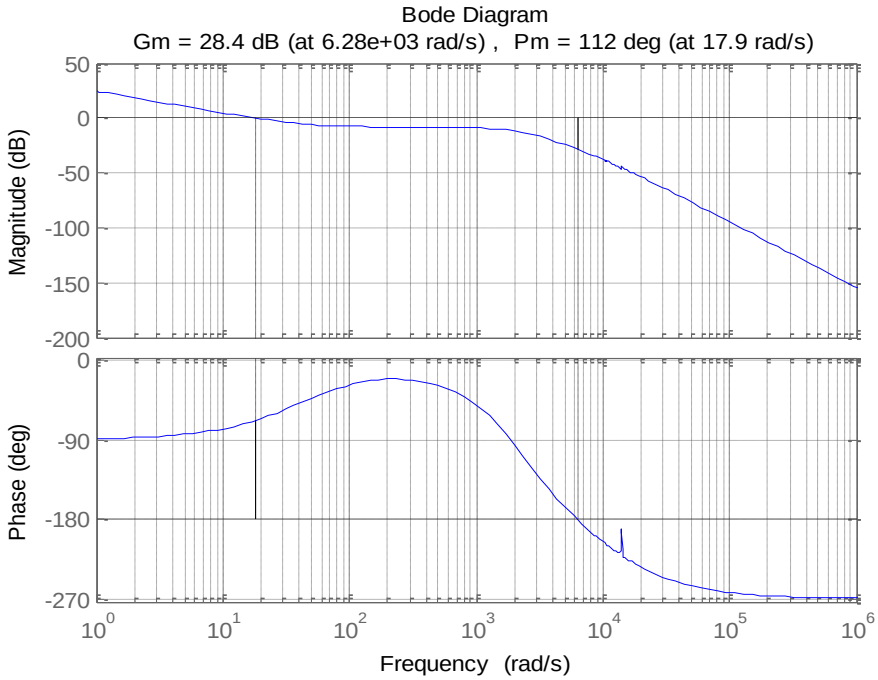


Figure 7.7: Bode plot of compensated transfer function $G_{vd}^{/}(s) * G_c(s)$

The Bode plots of uncompensated transfer functions, $G_{vd}(s)$ and $G_{vd}^{/}(s)$ are shown in figure 7.5 and figure 7.6 respectively. It may be seen from figures 7.5 and 7.6 that the Bode plots are almost identical. As may be seen from Bode plot in figure 7.7, the converter system is stable even after the introduction of an input filter. These Bode plots further verify the efficacy of the extra element theorem based methodology in determining the converter transfer function after introduction of an input filter. These plots also verify the significance of the necessary inequalities, (7.29) and (7.30) that are to be considered for the design of the input filter for Center-Point-Clamped AC-AC Converter in order to preserve the performance and stability of the converter system.

It has been verified that the Bode plot of the converter transfer function derived in Section 7.4 is same as the Bode plot of the converter transfer function obtained in this section through the above discussed Extra Element theorem. This further validates the

implementation of the technique discussed in this section to obtain the converter transfer function when an input side filter or an extra element is added to a converter.

CHAPTER 8 : SIMULATION RESULTS

8.1. Introduction

In this chapter, simulation results' verifying the operation and efficacy of the proposed Center-Point-Clamped AC-AC Direct Power Converter has been presented. Single phase ($2.4kV_{line\text{-}neutral}$) of the proposed converter for $4.16kV_{line\text{-}line}$, 600 kW application has been simulated using Matlab/Simulink. The IGBT switches have been considered to be ideal in the Simulink model. A simplified circuit schematic of the converter has been shown in figure.8-1.

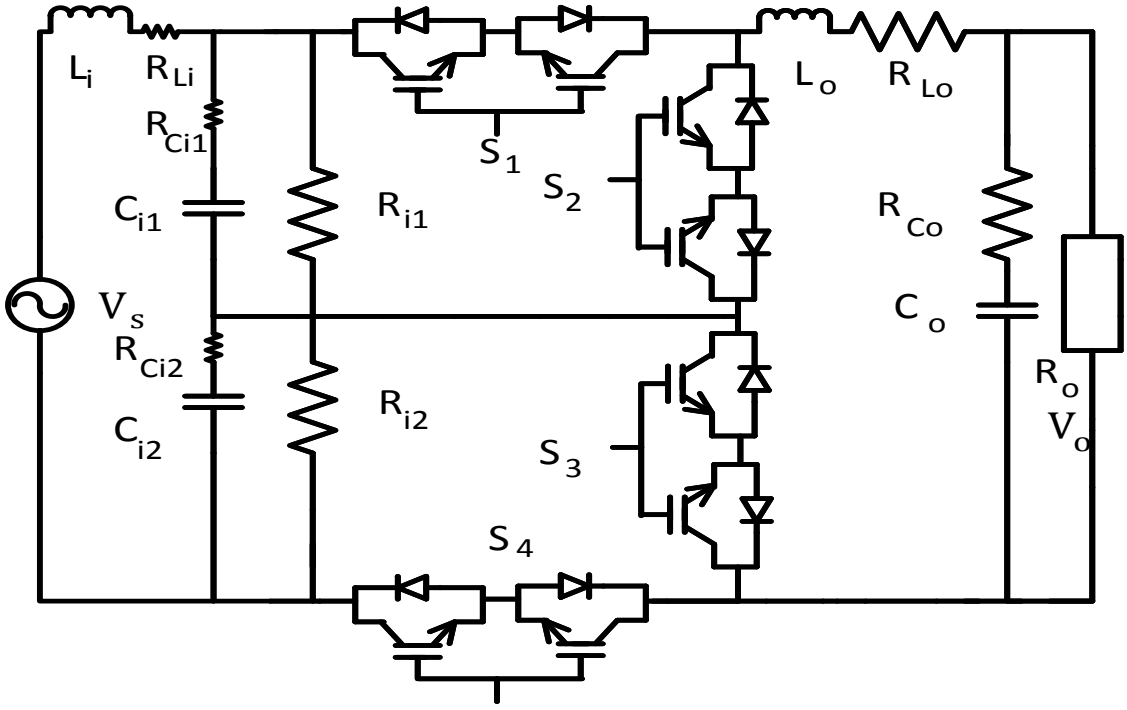


Figure 8.1: Simplified circuit schematic of center-point-clamped ac-ac buck converter with input filter.

It may be seen from figure 8.1 that the input side inductor has been included in the simulation model. The design parameters for the simulation model have been discussed in the following sections.

8.2. Matlab-Simulink Model of Center-Point-Clamped AC-AC Converter

The matlab-simulink model of the proposed converter has been designed using the simulation parameters tabulated in Table 3.

Table 3. Simulation Parameters

$V_{line\text{-}line}$	4160 V rms
$P_{3\text{-}\varphi}$	600 kW
v_{in}(line-neutral)	2400 V rms
L_i	0.1e-3 H
R_{Li}	10e-3 Ω
R_{i1}, R_{i2}	3e+3 Ω
C_{i1}, C_{i2}	100e-6 F
R_{Ci1}, R_{Ci2}	1e-3 Ω
L_O	20.5e-3 H
R_{LO}	2.2e-3 Ω
C_o	300e-6 F
R_{Co}	2.75e-3 Ω
f_{sw}	1.2kHz

The design of the simulation parameters have been analyzed in Chapter 6 and Chapter 7. The switching sequence for the proposed converter has already been discussed in Section 3.3. It may be seen from the simulation results that the switching sequence proposed for the center-point-clamped ac-ac buck converter implements input side capacitor voltage balancing as discussed in Section 3.4. A screenshot of the Matlab-Simulink model of the center-point-clamped ac-ac buck converter is shown in figure 8.2.

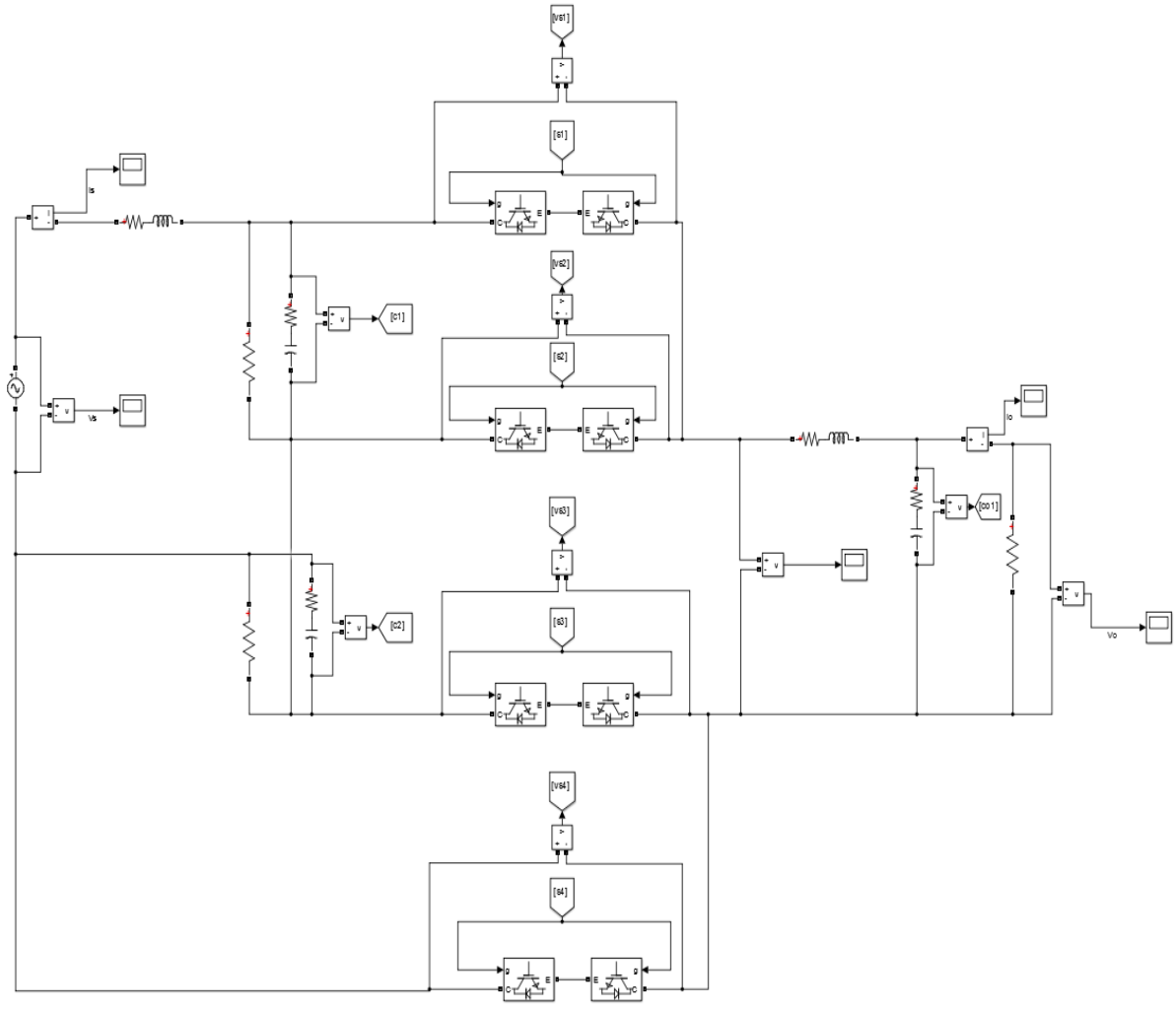


Figure 8.2: Matlab-Simulink model of center-point-clamped ac-ac buck converter with input filter.

8.3. Operational Simulation Results

The modulation strategy of the converter may be seen from Table 1. The operational simulation results have been shown for v_{oref} = 0.3v_{in} and v_{oref} = 0.8v_{in}. As may be observed from figure 8.3, when desired output peak voltage is less than 0.5v_{in}, the converter switches between 0 and v_{in}/2 sinusoidal waveform. Alternatively, it may be seen in figure 8.4 that, when desired output peak voltage is more than 0.5v_{in}, the converter switches between v_{in}/2 and v_{in} sinusoidal waveforms. This method of operation offers superior spectral performance compared to conventional ac-ac buck converter which switches between 0 and v_{in}.

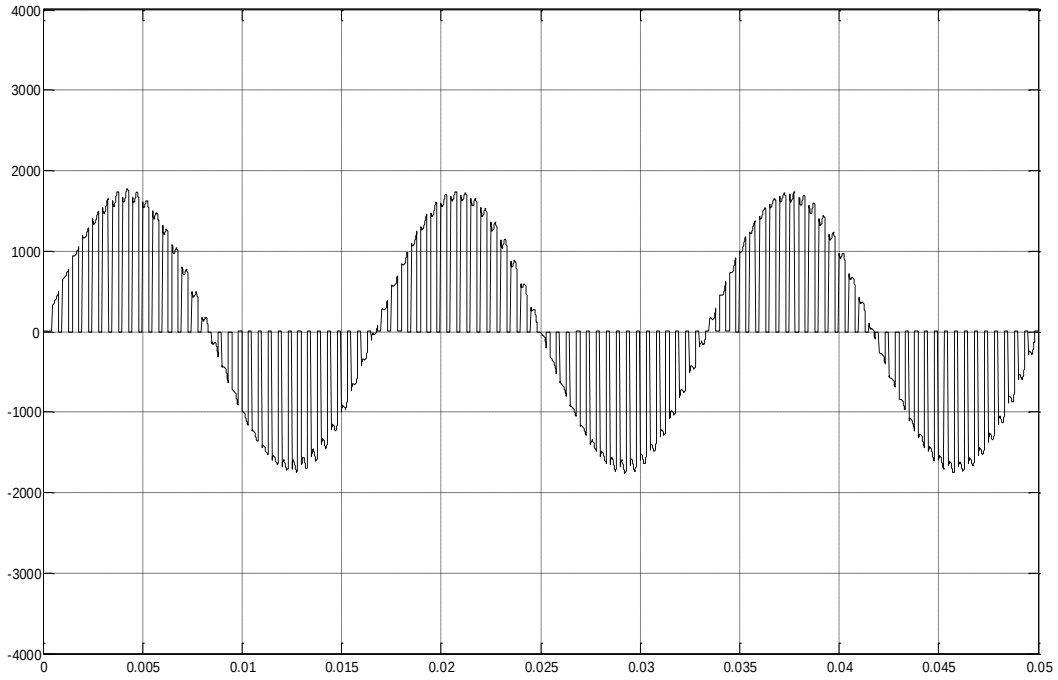


Figure 8.3: Unfiltered Output Voltage waveforms when v_{oref} = 0.3v_{in}

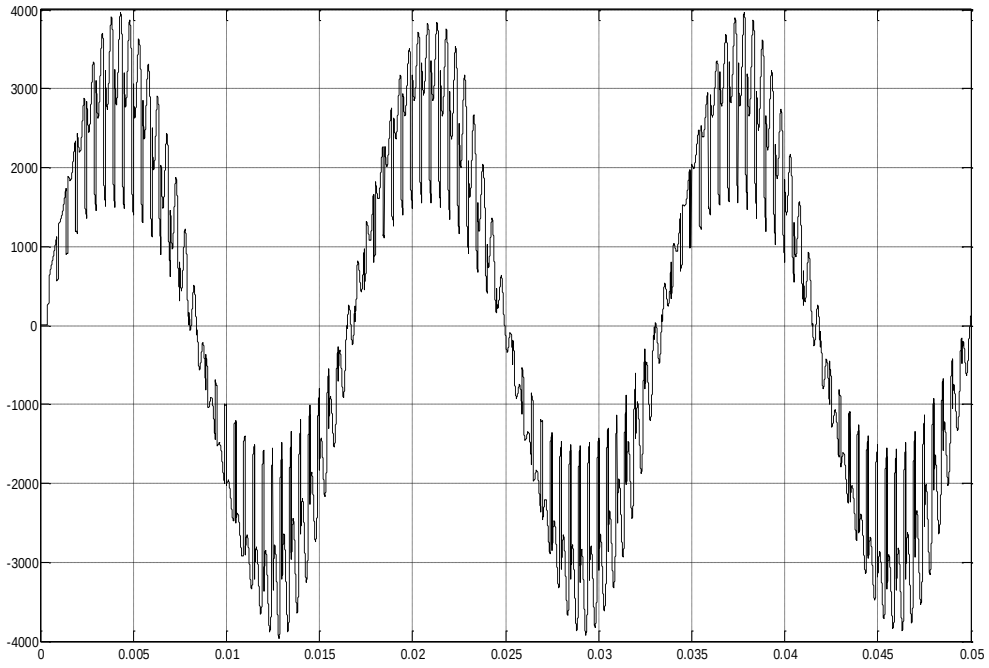


Figure 8.4: Unfiltered Output Voltage waveforms when v_{oref} = 0.8v_{in}

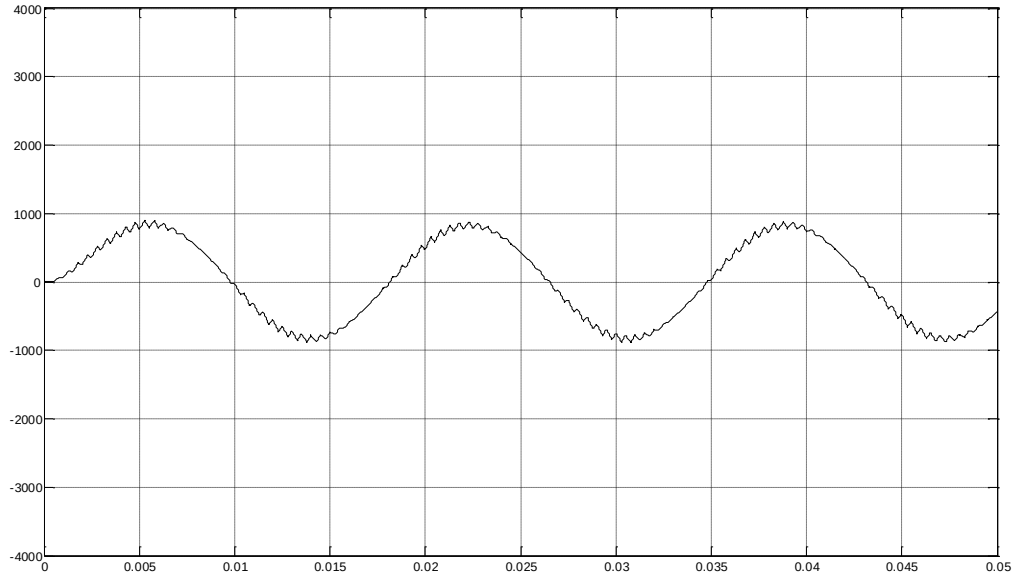


Figure 8.5: Filtered Output Voltage waveforms when v_{oref} = 0.8v_{in}

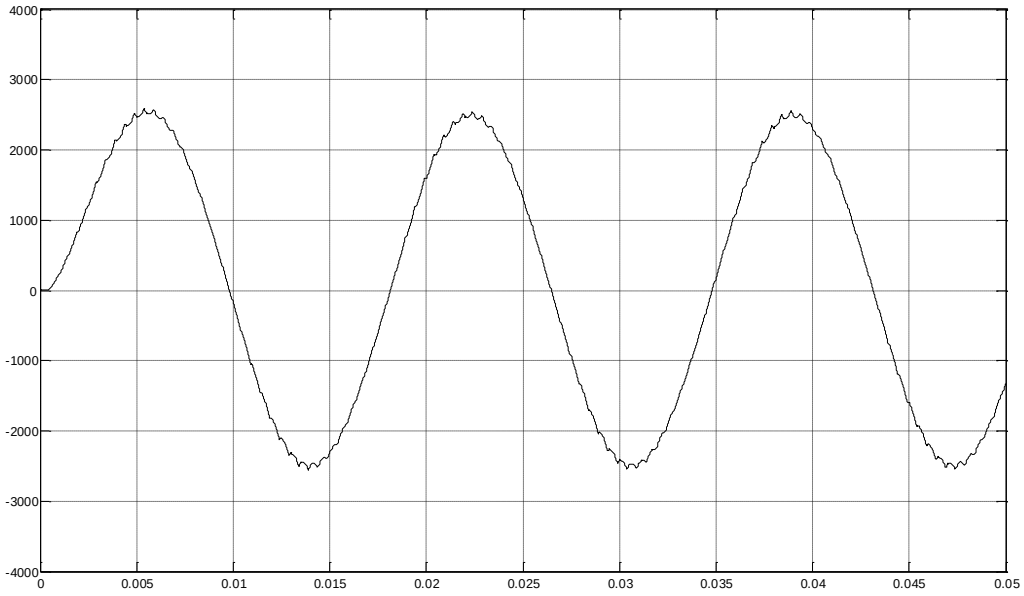


Figure 8.6: Filtered Output Voltage waveforms when v_{oref} = 0.8v_{in}

It may be observed from figures 8.5 and 8.6 that the low pass output filter designed for the converter in Chapter 5 has removed the high frequency switching harmonics that may be seen in figures 8.3 and 8.4. Furthermore, it may also be seen from figures 8.7 and 8.8 that under all conditions, voltages across all switches are clamped to v_{in}/2 with the proposed topology. This verifies the implementation of the concept of input side capacitor voltage balancing as discussed in Section 3.4. Thus, it may be said that switches rated at half the input voltage can be used to implement the center-point-clamped ac-ac buck converter, thereby increasing the efficacy of the converter as compared to other prevalent ac-ac converter topologies which require switches rated at the input voltage.

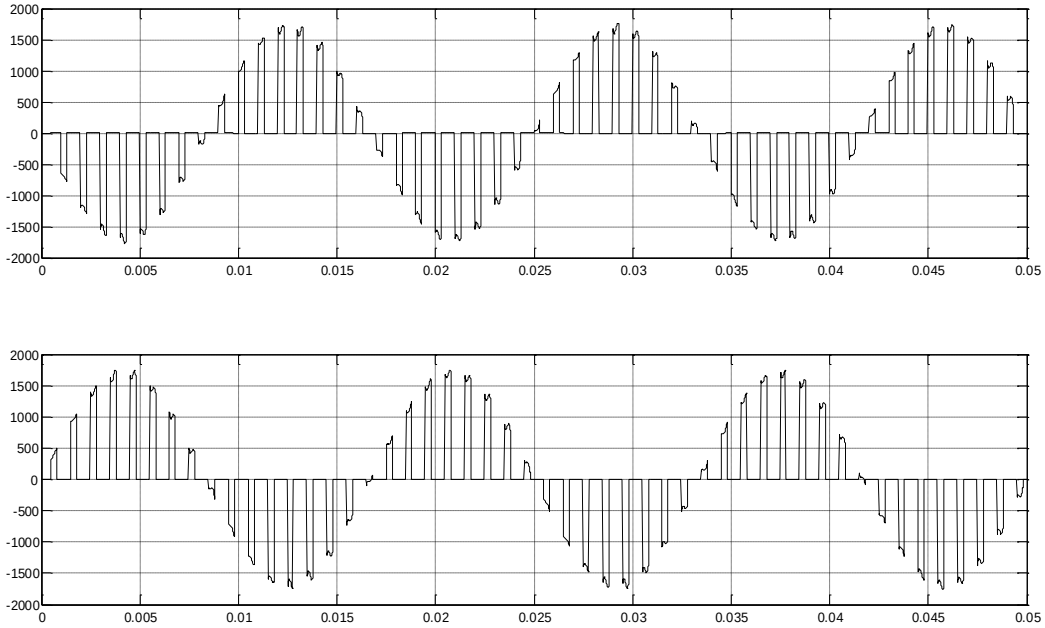


Figure 8.7: Voltages across S2 and S3

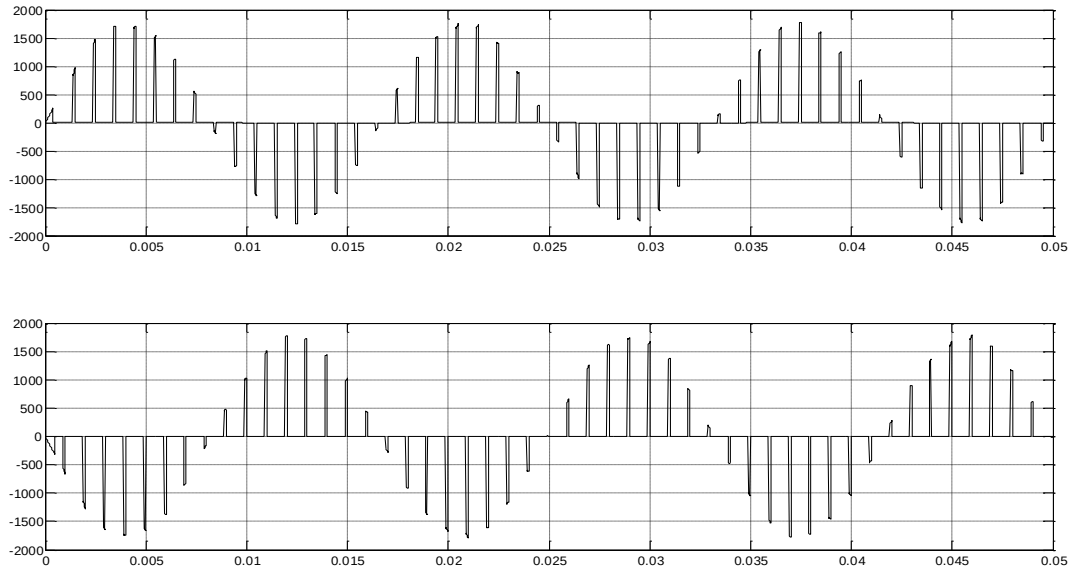


Figure 8.8: Voltages across S_1 and S_4

8.4. Open Loop Simulation Results

The open loop simulation results comprise of the simulation results obtained without the implementation of the feedback compensator. These simulation results have been analyzed in this section. It may be seen from figures 8.9 and 8.10 that the filtered output voltage and current have negligible higher switching harmonics.

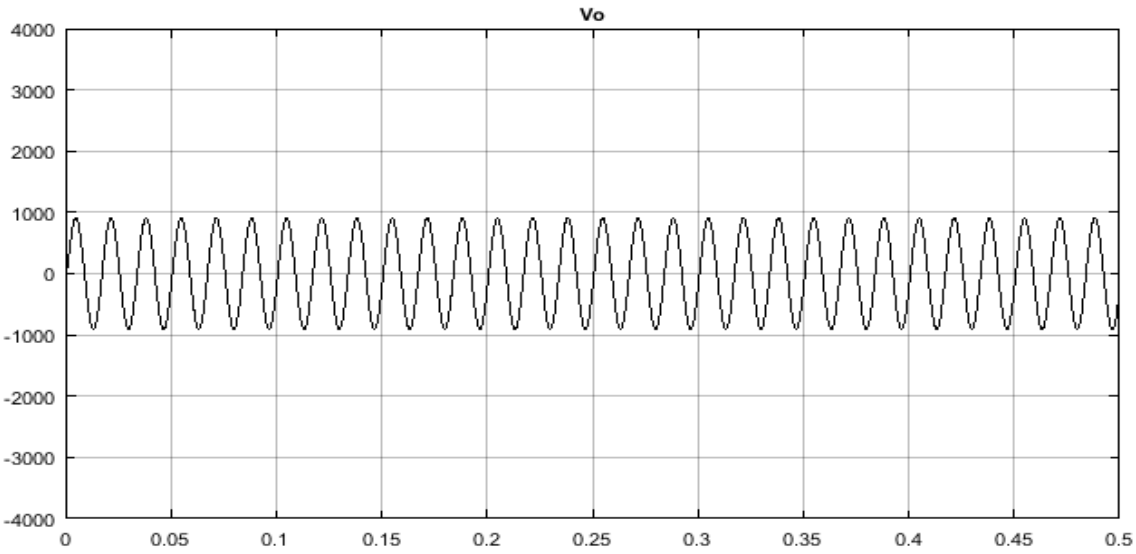


Figure 8.9: Filtered output voltage waveform for D=0.25

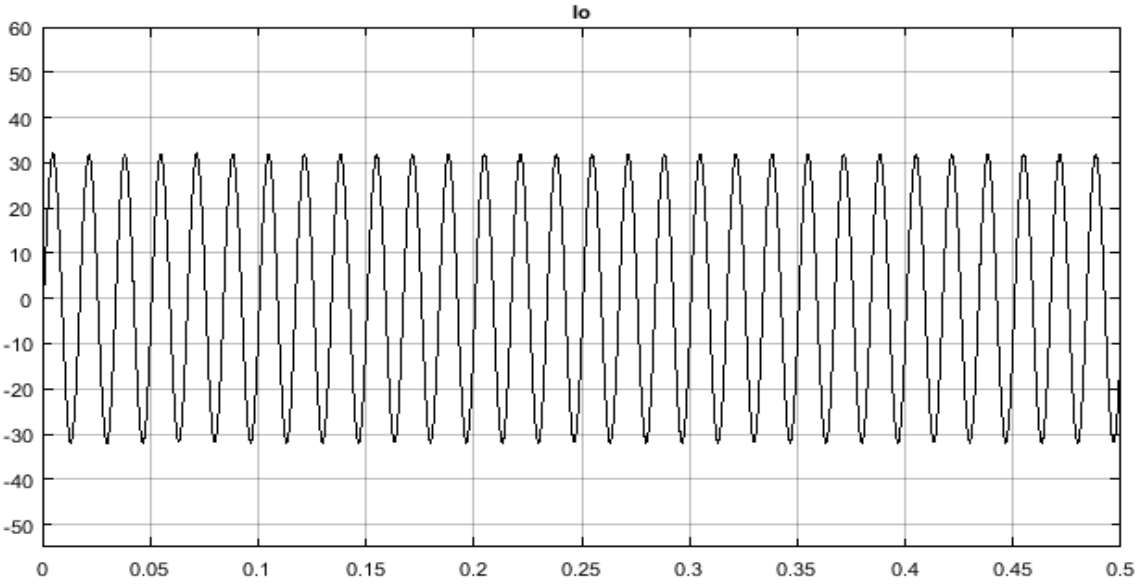


Figure 8.10: Filtered output current waveform for D=0.25

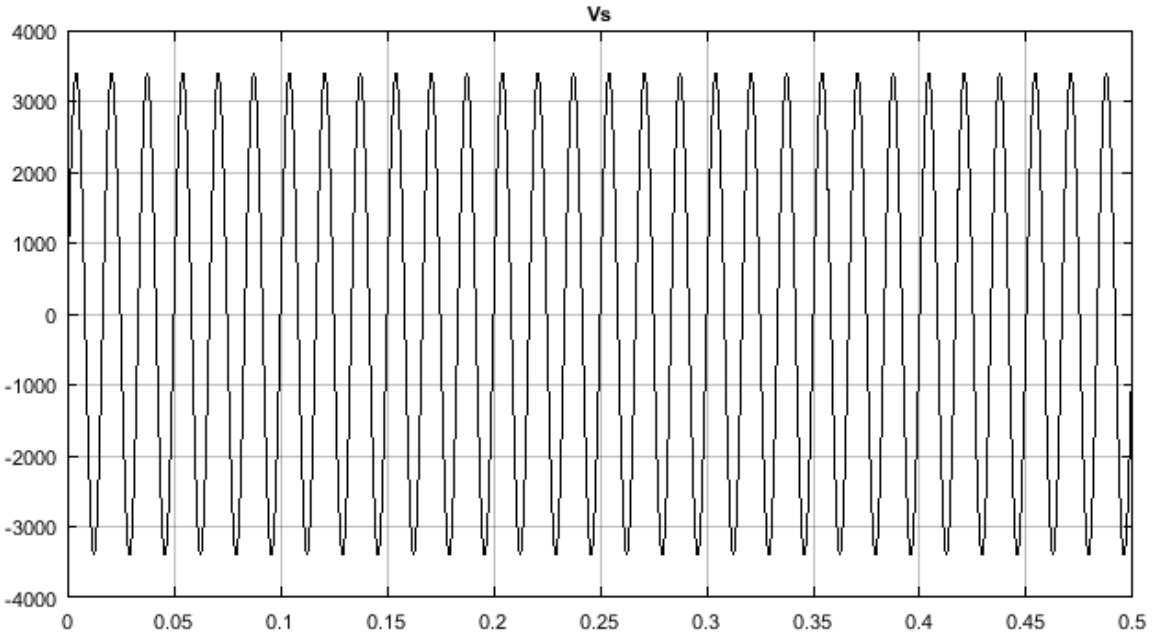


Figure 8.11: Input source voltage waveform for D=0.25

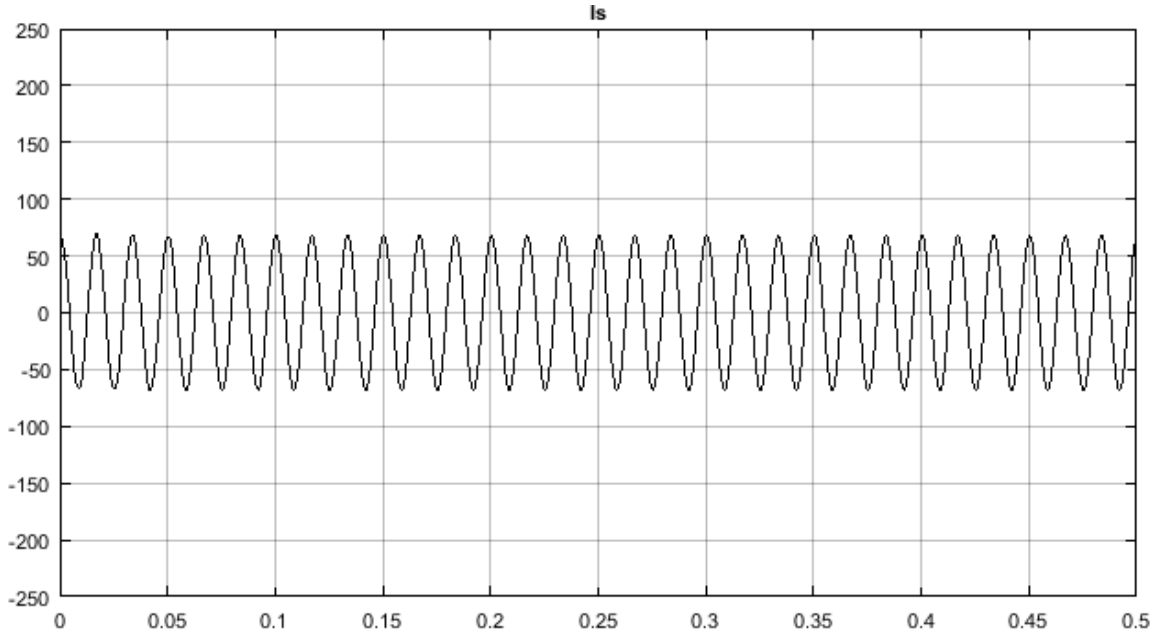


Figure 8.12: Waveform of input current drawn from the source for D=0.25

It may be seen from figures 8.11 and 8.12 that the designed input filter has removed the higher frequency current harmonics from being introduced into the unregulated power supply.

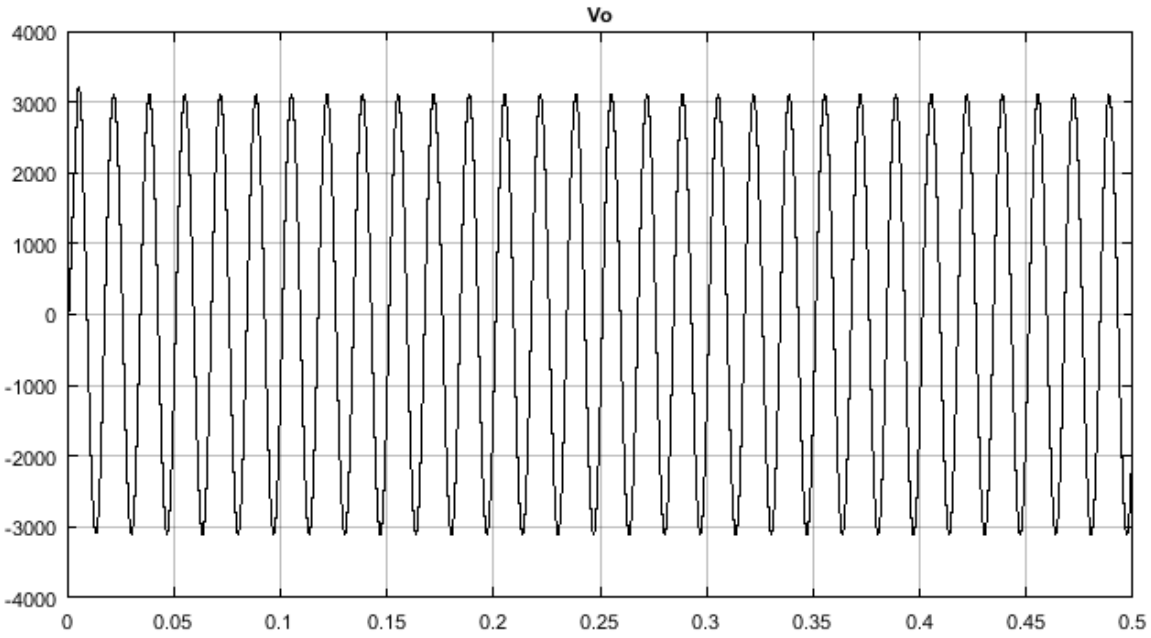


Figure 8.13: Filtered output voltage waveform for D=0.75

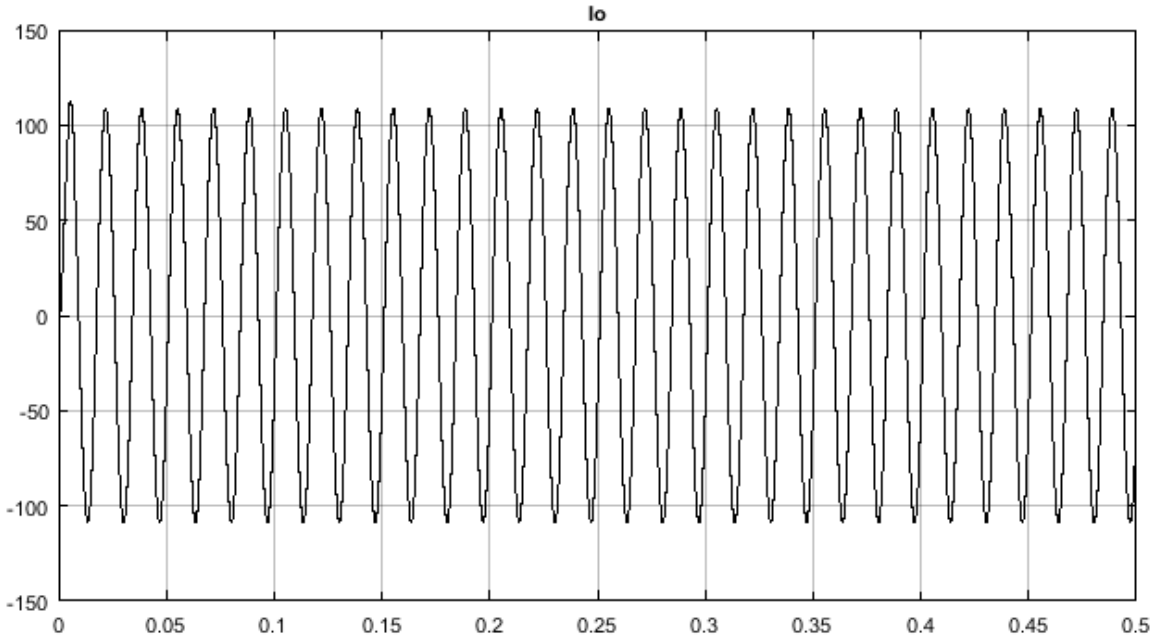


Figure 8.14: Filtered output current waveform for D=0.75

Simulation results shown in figures 8.13 and 8.14 verify the efficacy of the designed output filter in Region 2 ($v_{in}\ to\ v_{in}/2$) of converter operation.

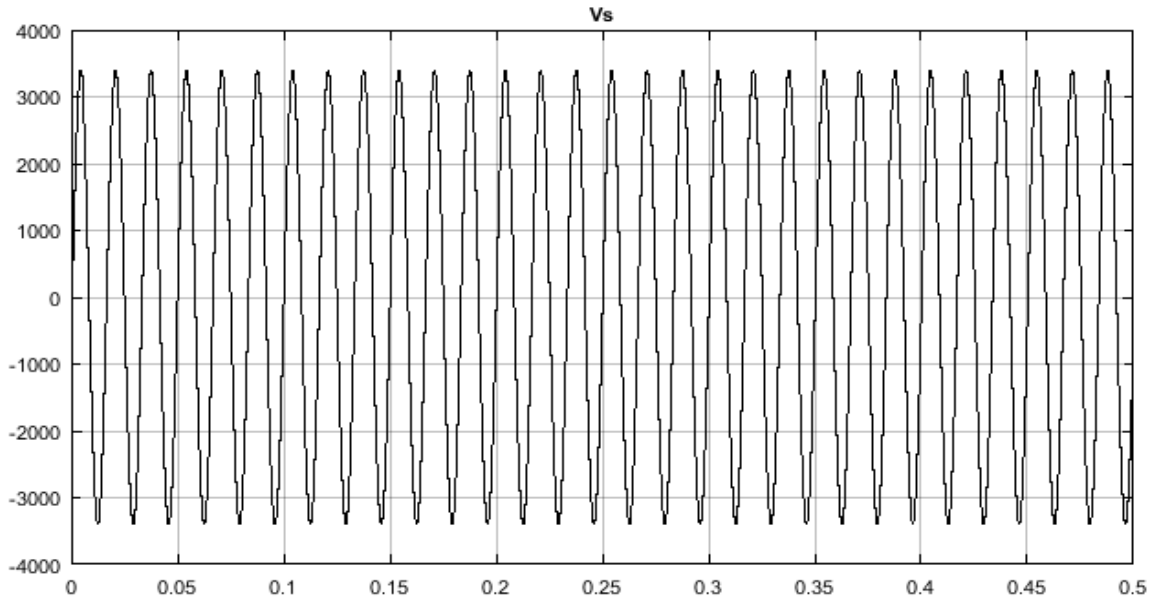


Figure 8.15: Input source voltage waveform for D=0.75

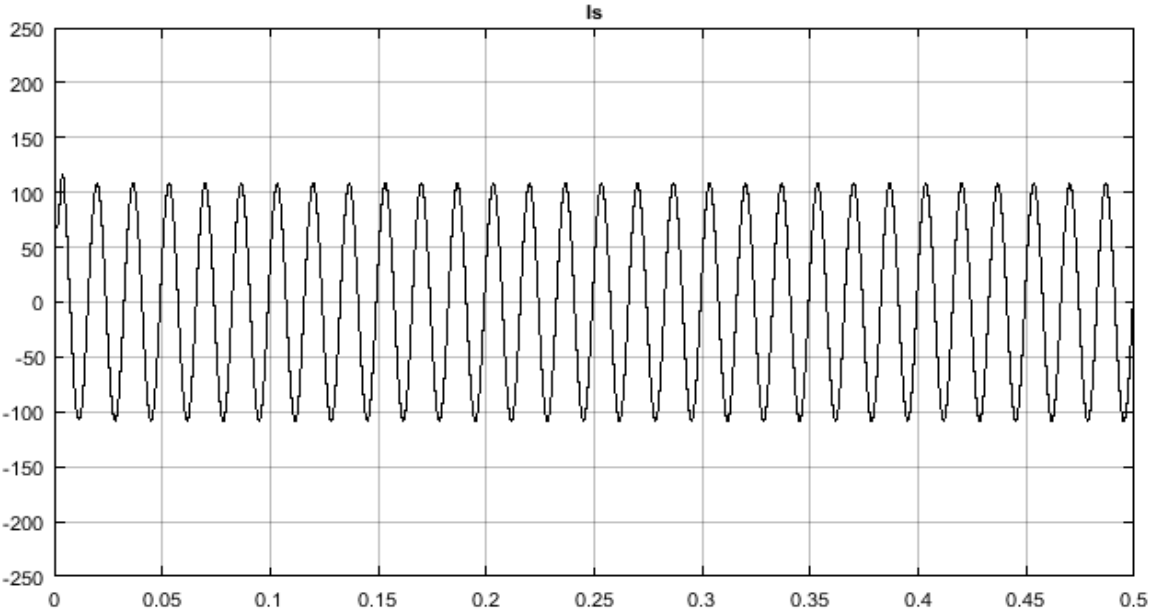


Figure 8.16: Waveform of input current drawn from the source for D=0.75

Simulation results shown in figures 8.15 and 8.16 demonstrate the effectiveness of input filter in eliminating the unwanted higher order frequency harmonics from being fed into the unregulated power supply in case of Region 2 ($v_{in}\ to\ v_{in}/2$) of converter operation.

8.5. Closed Loop Simulation Results

The command following performance of the feedback compensator designed for the center-point-clamped ac-ac buck converter may be analyzed through figures 8.17 and 8.18.

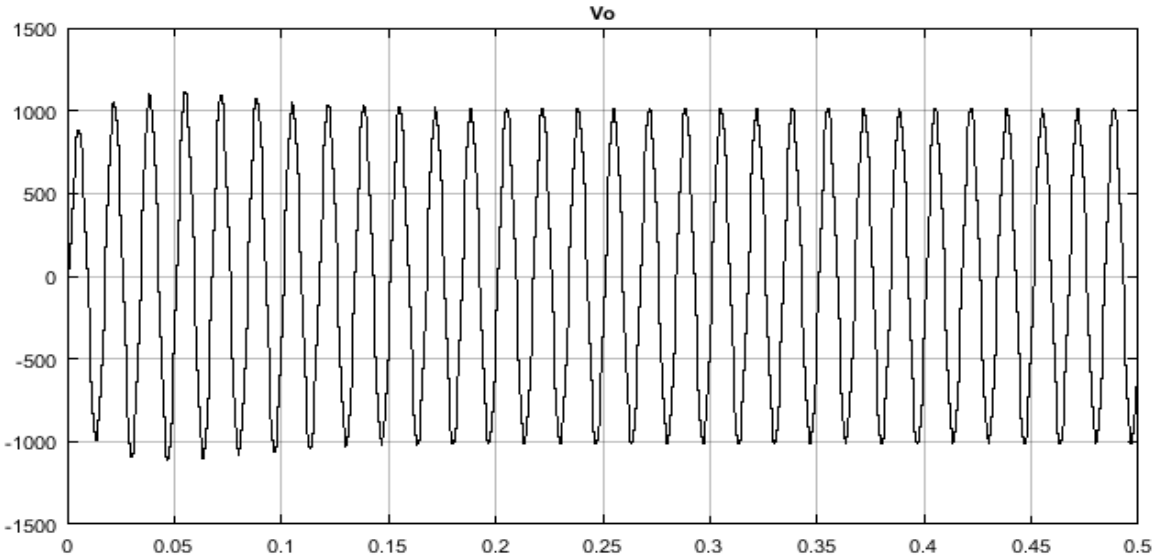


Figure 8.17: Filtered output voltage waveform for v_{oref} = 1000V

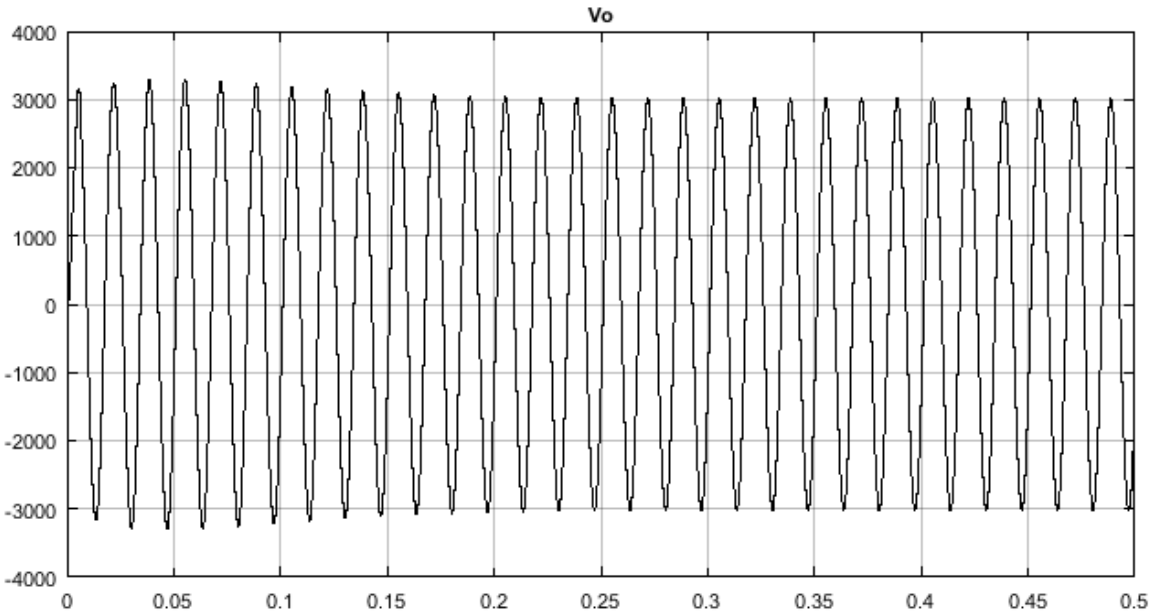


Figure 8.18: Filtered output voltage waveform for v_{oref} = 3000V

To illustrate the dynamics associated with feedback control, first change of operating point is simulated as follows:

In Region 1, initially the operating point is set at v_{oref} = 1000V. After system reaches 1000V, the operating point is moved within same Region 1 to 1500V at 0.2 sec. This is shown in figure 8.19.

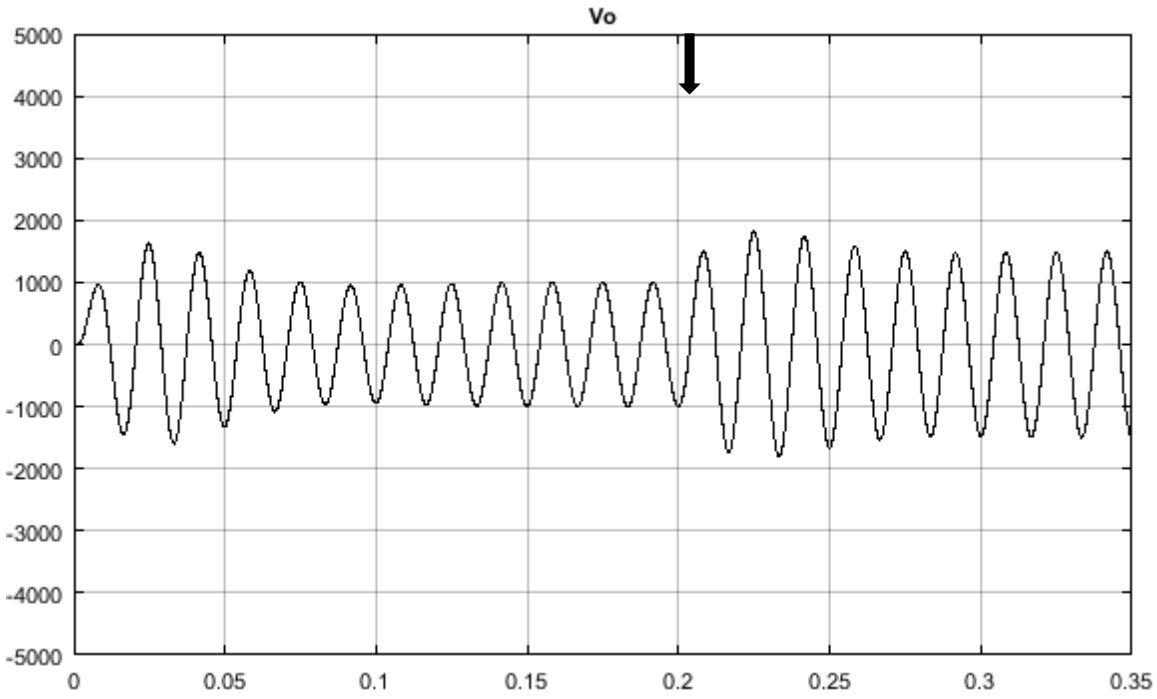


Figure 8.19: Change of operating point within Region 1 (1000V to 1500V)

In Region 2, initially the operating point is set at v_{oref} = 2500V. After system reaches 2500V, the operating point is moved within same Region 2 to 3000V at 0.2 sec. This is shown in figure 8.20.

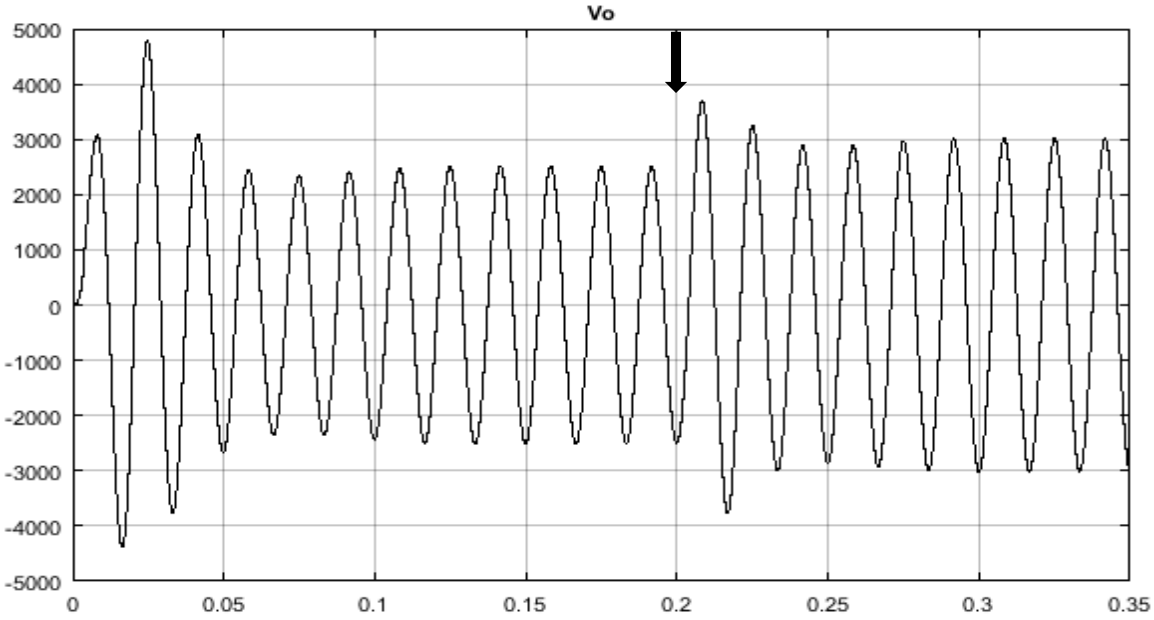


Figure 8.20: Change of operating point within Region 2 (2500V to 3000V)

Finally, in Region 1, initially operating point is set at v_{oref}= 1500V. After system reaches 1500V, operating point is moved to Region 2 to 3000V at 0.2 sec. This is shown in figure 8.21.

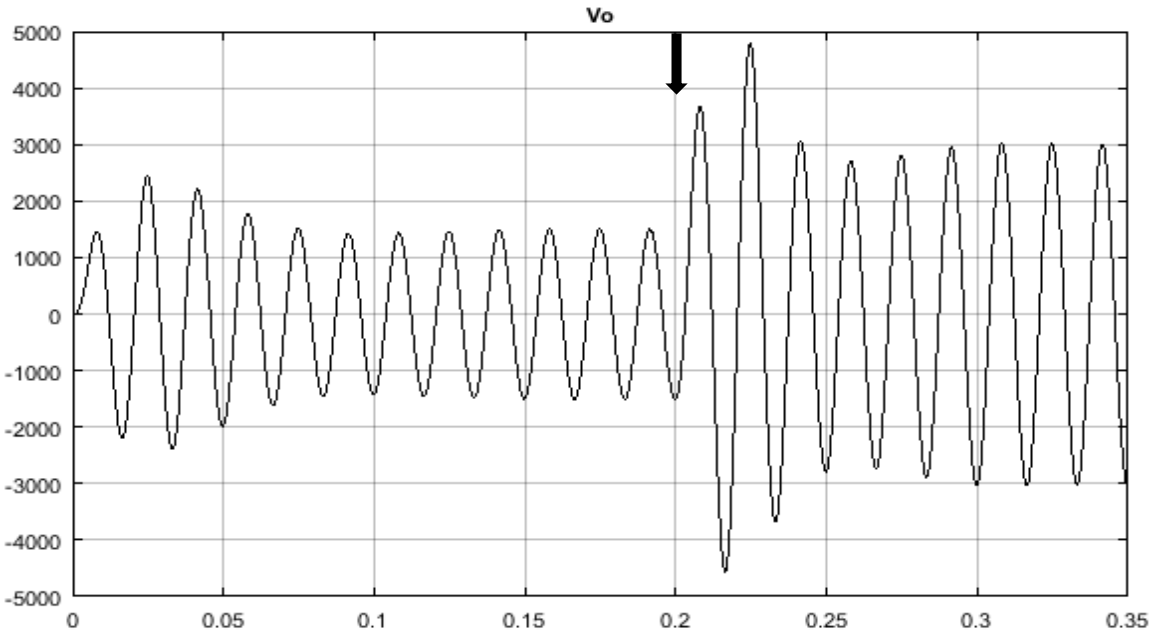


Figure 8.21: Change of operating point from Region 1 (1500V) to Region 2 (3000V)

As may be seen from figures 8.19, 8.20, and 8.21, upon change of reference, the output voltage exhibits a small overshoot and then settles to the new value in two-three fundamental cycles. This also illustrates the efficacy of the designed feedback compensator in following the command reference input.

To evaluate the line regulation performance of center-point-clamped ac-ac direct converter under varying source voltages, input voltage is varied by +10% and –10% of 3400V. First, this line voltage is increased by 10% at 0.2 sec, and its effect on the output voltage waveform is shown in figure 8.22.

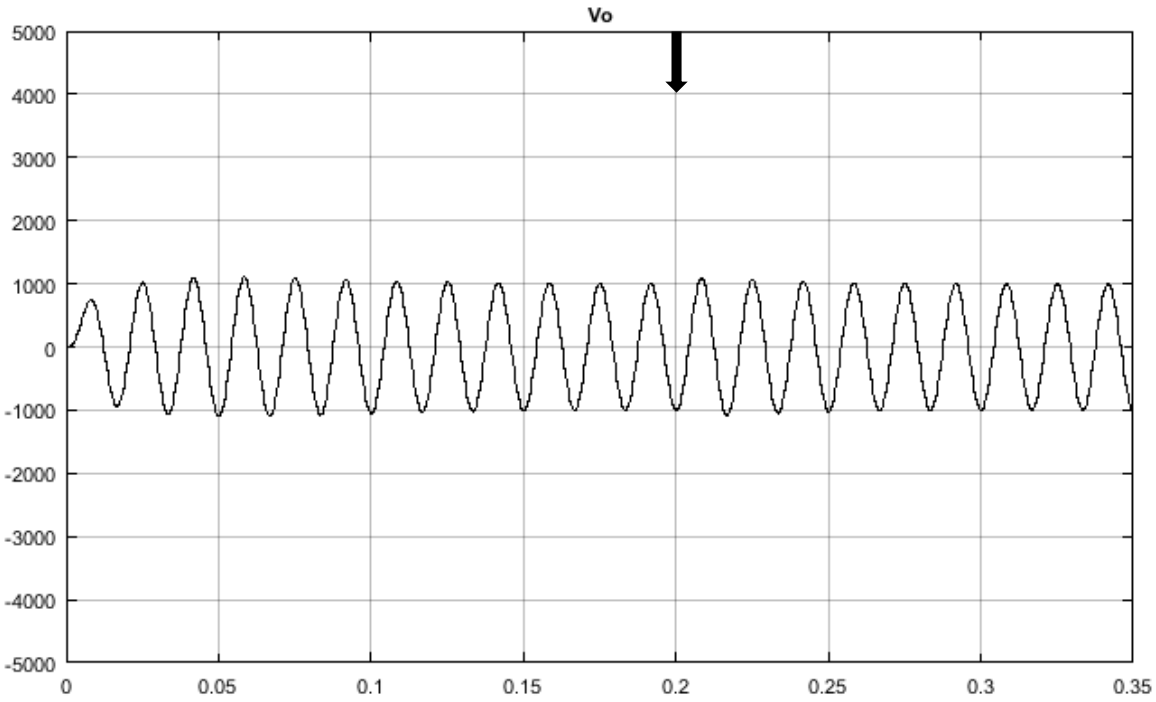


Figure 8.22: Line regulation: performance during 10% increase in line voltage

Next, the line voltage is decreased by 10% at 0.2 sec, and its effect on the output voltage waveform is shown in figure 8.22.

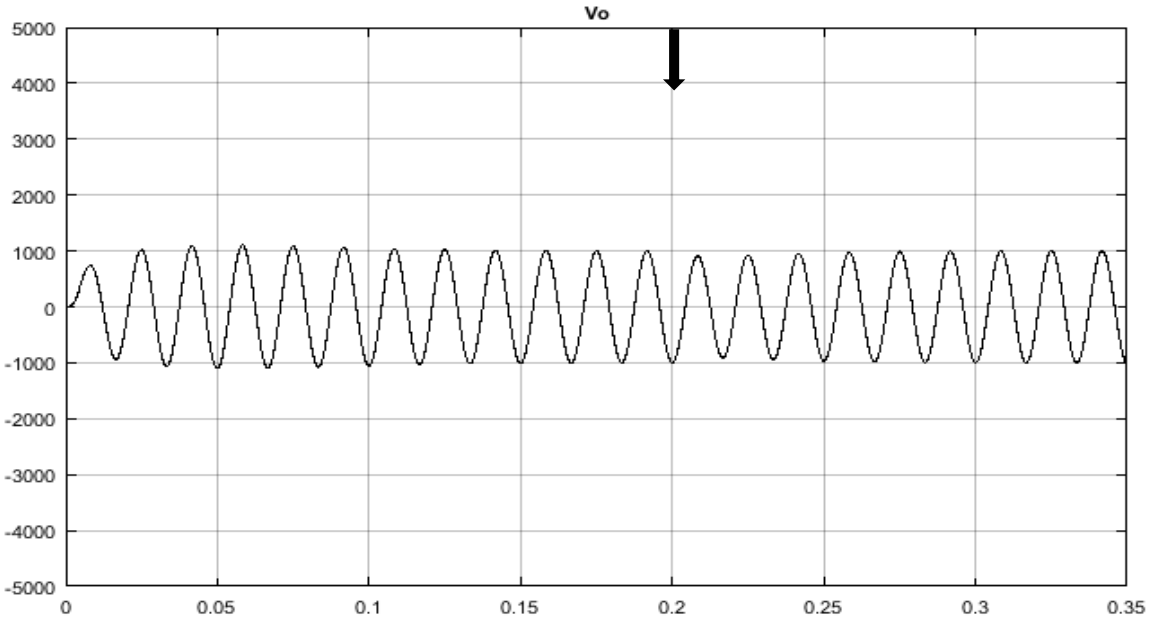


Figure 8.23: Line regulation: performance during 10% decrease in line voltage

As may be seen from figure 8.22, when the line voltage experiences a spike of 10%, the output voltage exhibits a minimal change. Similarly, as illustrated in figure 8.23, when the line voltage experiences sag of 10%, the output voltage exhibits a negligible effect. This illustrates the command following performance of the system.

Finally, to evaluate the load regulation performance of center-point-clamped ac-ac converter under varying load currents, output current is varied by +50% and –50% of 35A . First, this load voltage is decreased from full load by 50%, and its effect on the output voltage waveform is shown in figure 8.24.

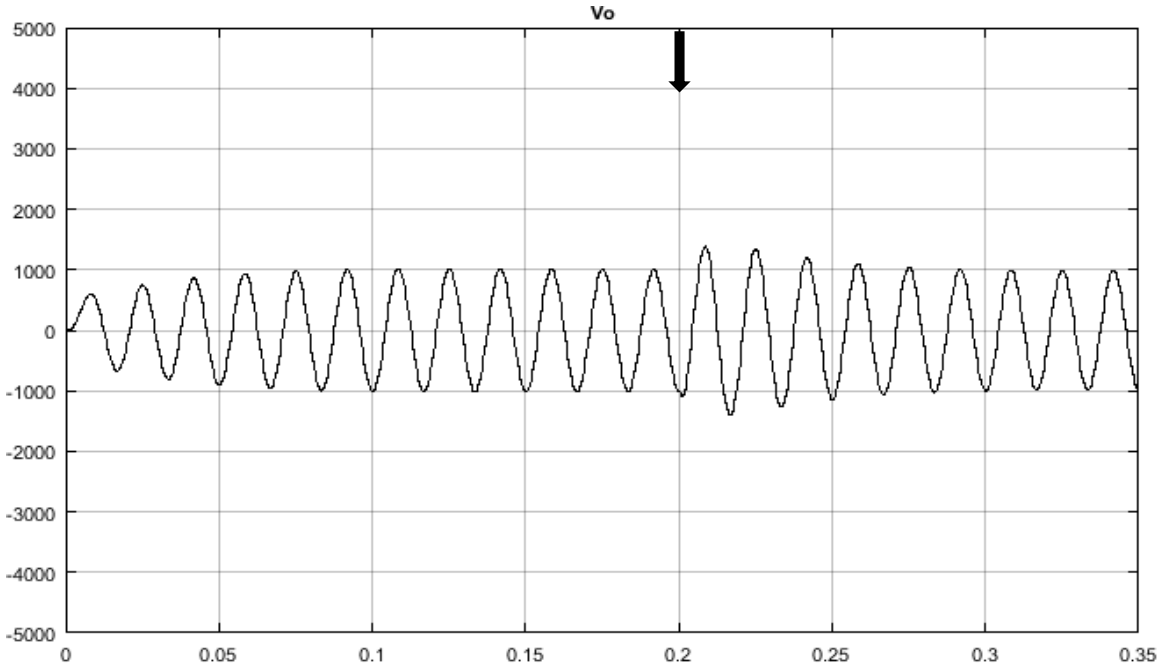


Figure 8.24: Load regulation: performance during 50% decrease in load current.

Next, load current is increased from 50% to full load, and its effect on the output voltage waveform is shown in figure 8.25.

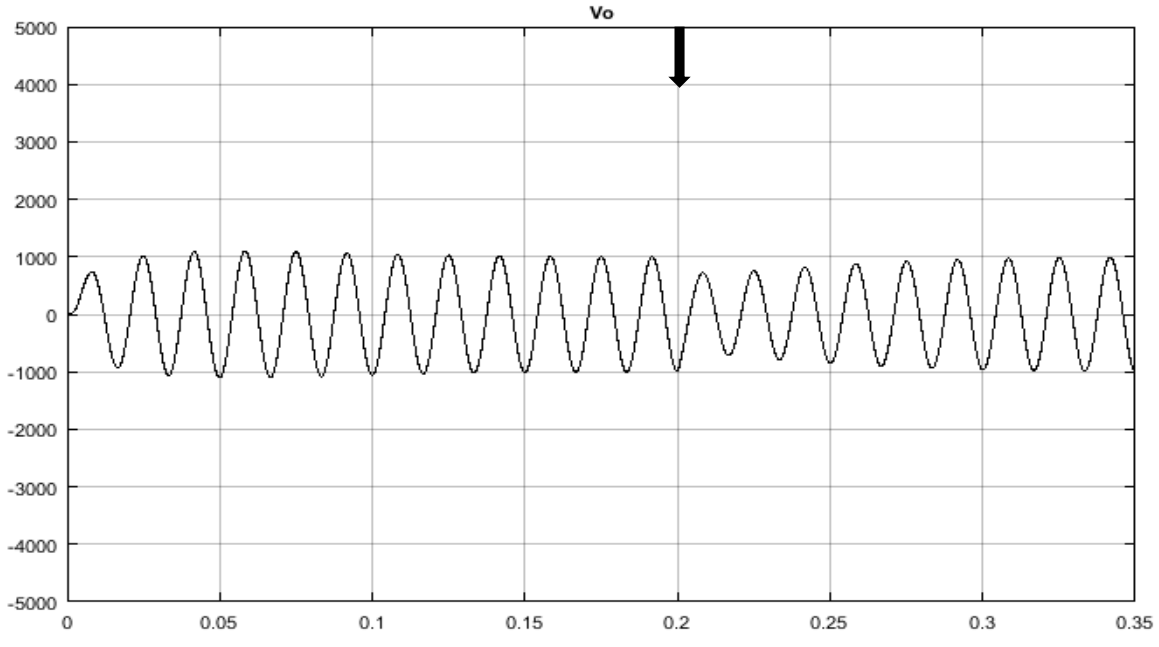


Figure 8.25: Load regulation: performance during 50% decrease in load current.

As may be seen from figure 8.24, when the load drops 50% at 0.2 sec, the output voltage exhibits a small overshoot and then decreases to the original value in two-three fundamental cycles. Similarly, when the load suddenly increases by 50% at 0.2 sec, the output voltage exhibits a small undershoot and then increases to the original value in two-three fundamental cycles. This is illustrated in figure 8.25. Thus, it may be observed that the center-point-clamped ac-ac buck converter reduces the voltage stress across the bi-directional switches, thereby facilitating the use of low rated power semiconductor devices for higher rated voltages. Also, it may be seen that the designed input filter eliminates the injection of higher order frequency harmonic current into the input side. Furthermore, it also verifies the efficacy of the command following performance of the designed feedback compensator.

CHAPTER 9 : EXPERIMENTAL RESULTS

9.1. Introduction

An experimental prototype has been built in the laboratory to illustrate the feasibility of the converter and verify the efficacy of feedback controller for the proposed Center-Point-Clamped AC-AC Buck Converter. Single phase ($120V_{line\text{-}neutral}$) of the proposed center-point-clamped ac-ac buck converter rated for $208V_{line\text{-}line}$, 10 kW applications has been constructed and tested. Experimental parameters are displayed in Table 4. The experimental set-up has been analyzed in the following section.

Table 4. Experimental parameters

$V_{line\text{-}line}$	208 V rms
$P_{3\text{-}\varphi}$	10 kW
v_{in}(line-neutral)	120 V rms
L_i	0.1e-3
R_{Li}	10e-3 Ω
R_{i1} , R_{i2}	3e+3 Ω
C_{i1} , C_{i2}	100e-6 F
R_{Ci1} , R_{Ci2}	1e-3 Ω
L_O	197e-6 H
R_{LO}	106e-3 Ω
C_o	3.5e-6 F
R_{Co}	2.75e-3 Ω
f_{sw}	20 kHz

9.2. Experimental Set-up Description

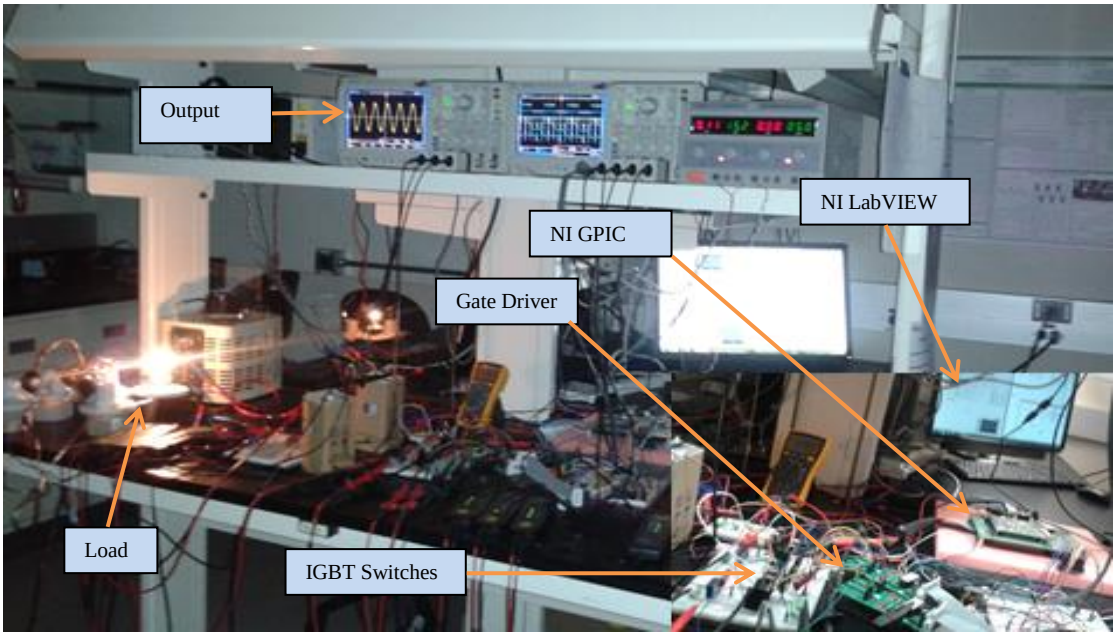


Figure 9.1: Picture of experimental prototype in the laboratory

A picture of the experimental prototype is shown in figure 9.1. The experimental set-up implements the center-point-clamped ac-ac buck converter using four bi-directional switches. Each bidirectional switch has been built using two IGBTs connected in anti-parallel fashion. The IGBT used in this set-up is IRGP4072DPbF, which is rated at 300V and 40A. The IGBT based bi-directional switches are driven by an isolated IGBT gate driver from CONCEPT Technologies, 2SC0106T2A0. This gate driver has been mounted on an interfacing base board also supplied by CONCEPT Technologies, 2BB0108T2A0. The gate drive pulses are supplied to the gate driver by National Instruments General Purpose Inverter Controller (GPIC). An interfacing circuitry acts as a buffer between the National Instruments (NI) GPIC and the gate driver to protect the NI GPIC against

current surge during fault conditions. The NI GPIC is an FPGA based controller designed by National Instruments (NI) mainly for quick prototyping of power electronic applications. The gate driver logic is designed using NI LabVIEW FPGA which is installed in the computer, as may be seen from figure 9.1. The designed NI LabVIEW program, popularly known as a Virtual Instrument (VI) is then compiled for errors and then on successful compilation, it is downloaded into NI GPIC. The NI GPIC has a base clock frequency of 40 MHz, which serves as the upper limit for the driver logic signal frequency. The concepts of instruction level parallelism may be introduced into the VI to run the driver logic signals on higher order frequency of clock signals.

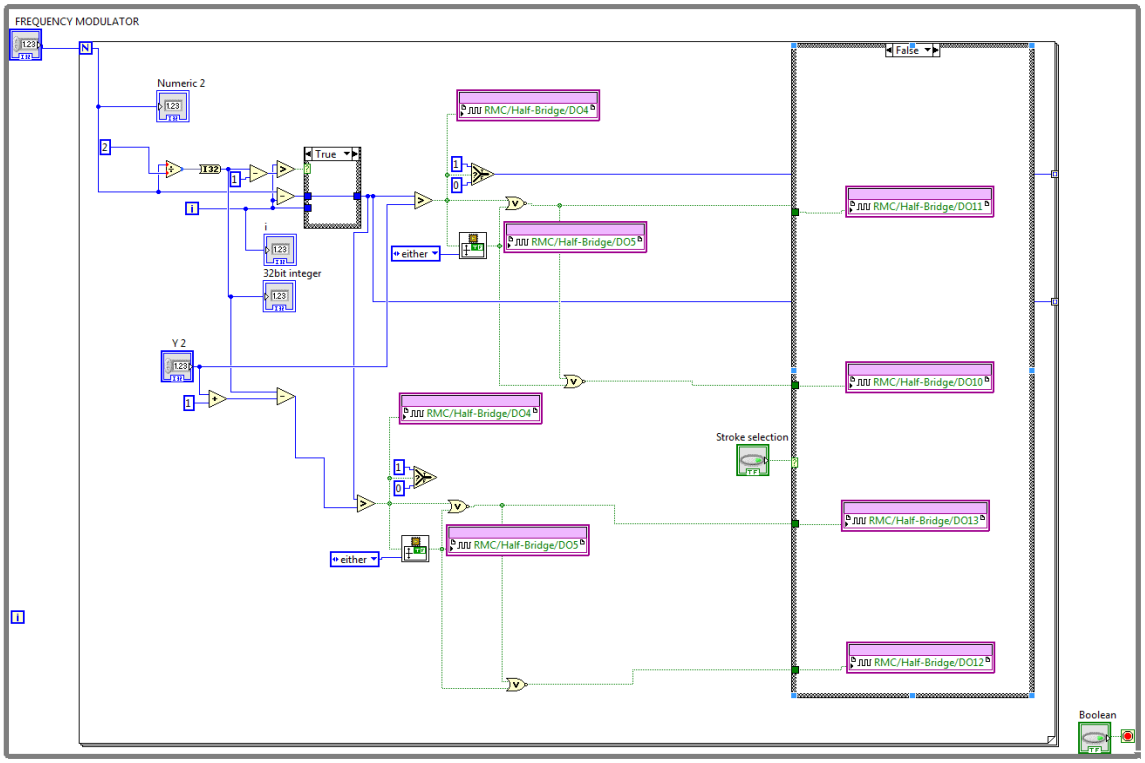


Figure 9.2: Picture of LabVIEW VI Block Diagram window implementing the gate driver logic

A picture of the LabVIEW VI generating the gate driver logic has been shown in figure 9.2. The modulation strategy described in Table 1 has been implemented in the

LabVIEW VI Block Diagram window shown in figure 9.2. As may be seen from figure 9.2, there is a Boolean stroke selection button which facilitates the change in the gate driver logic based on the operating point's location in the region (0 to v_{in}/2 or v_{in}/2 to v_{in}) of operation. It implies that when the desired output voltage lies between (0 to v_{in}/2), the LabVIEW VI generates the driver logic signals corresponding to the switching sequence for (0 to v_{in}/2) as shown in Table 1. Similarly, in case of desired output voltage between (0 to v_{in}/2), the LabVIEW VI generates the driver logic signals corresponding to the switching sequence for (v_{in}/2 to v_{in}) as shown in Table 1. The generated signals for the two regions of operation are shown in figure 9.3 and 9.4.

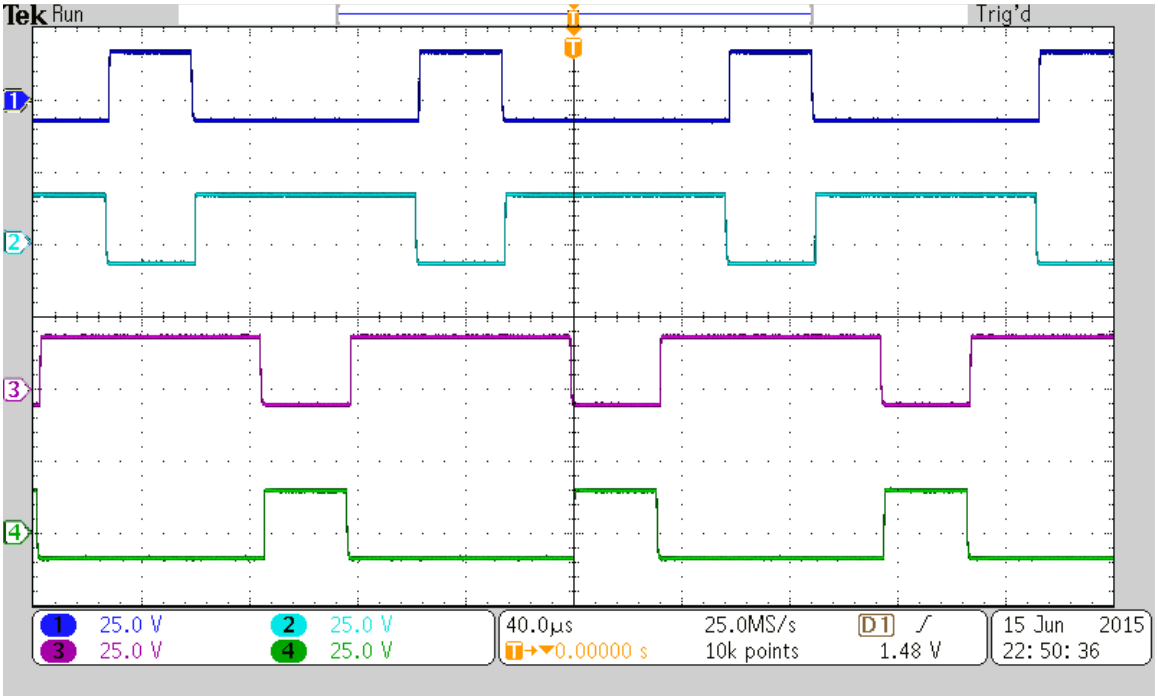


Figure 9.3: Driver Logic Signal waveform for switches, S_1, S_2, S_3, and S_4 when v_{oref}=0.3v_{in}

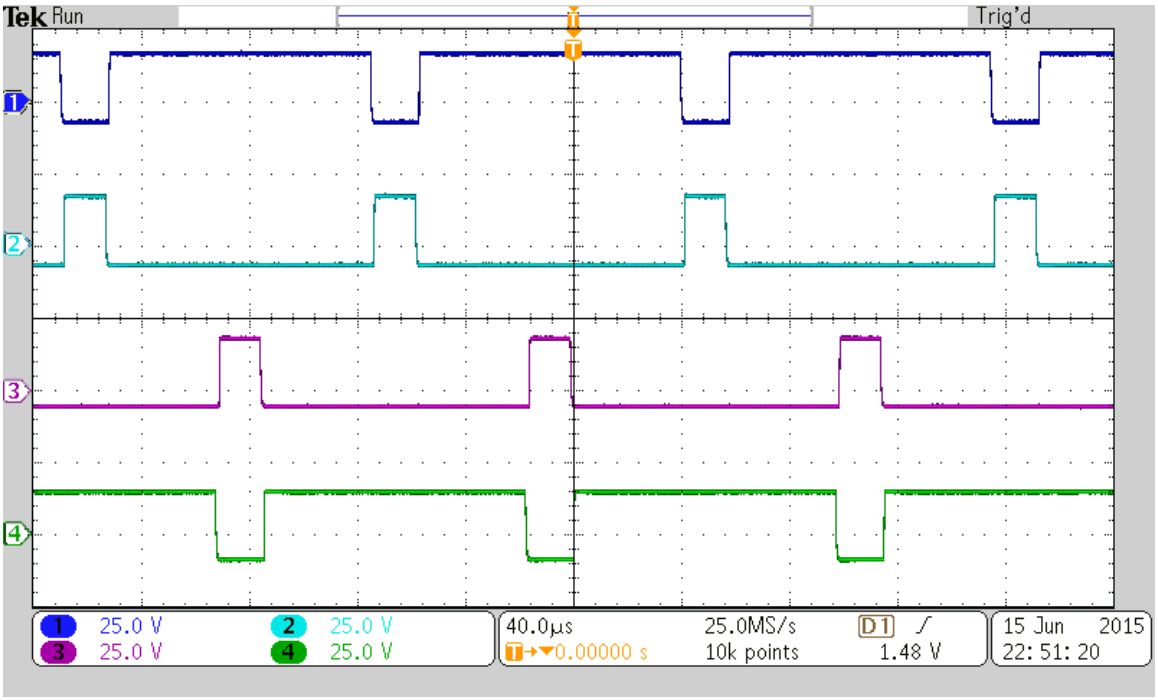


Figure 9.4: Driver Logic Signal waveform for switches, S_1, S_2, S_3, and S_4 when v_{oref}=0.8v_{in}

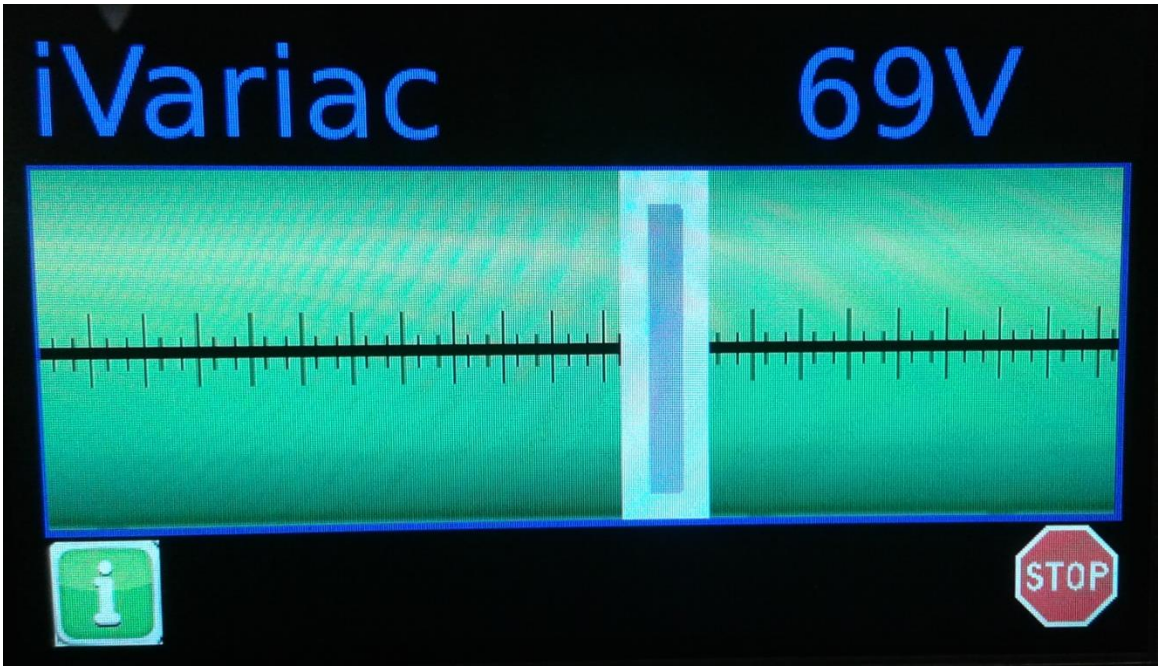


Figure 9.5: User Interface for entering reference output voltage, v_{oref} command input.

Figure 9.5 shows the capacitive touch screen based user interface from Reachtech Technologies. The User Interface has been designed using Query Mark-up Language (QML). The User Interface comprises of a horizontal slider which can be adjusted to the desired value using our fingertip. This slider input may be used to generate reference voltage values ranging from 0V to 120V rms. The slider input is sensed in a LabVIEW VI running in the computer. The User Interface data is transferred to the computer via serial communication protocols. This data is then taken as the reference output voltage, v_{oref} input by a LabVIEW VI, as shown in figure 9.6.

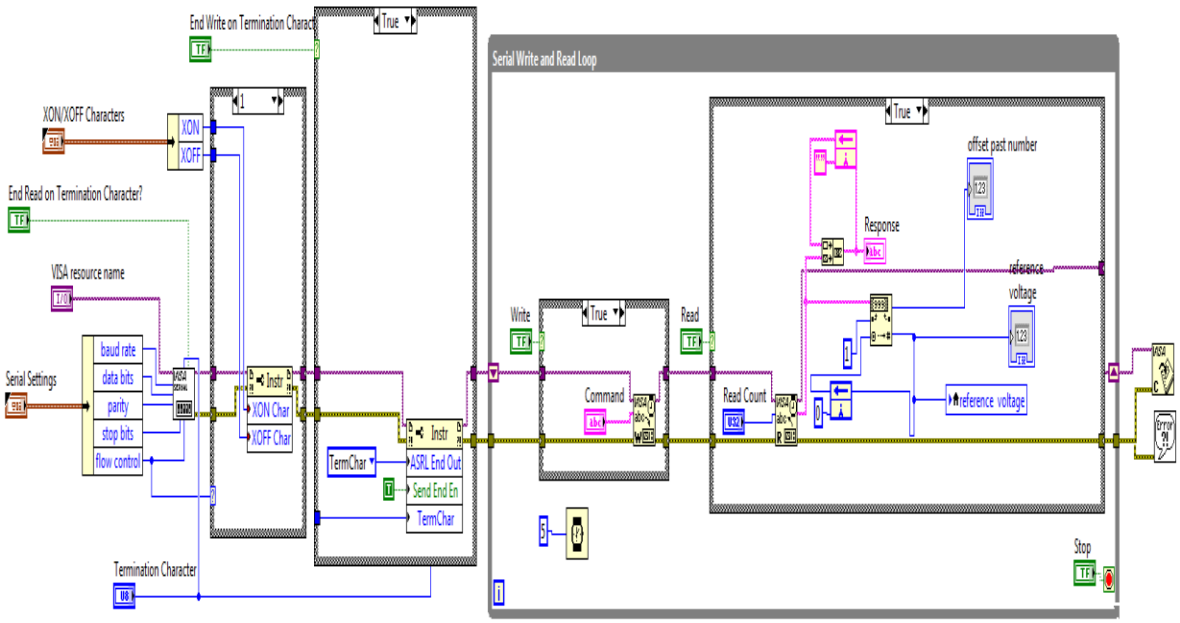


Figure 9.6: Picture of the LabVIEW VI sensing the reference output voltage, v_{oref} from the slider input

The output voltage, v_o is scaled down by a transformer having a transformation ratio of 10:1. The scaled down output voltage is then sensed by NI GPIC. The sensed output voltage is then sent to a Phase Locked Loop which has been implemented in a LabVIEW VI, as may be seen in figure 9.7.

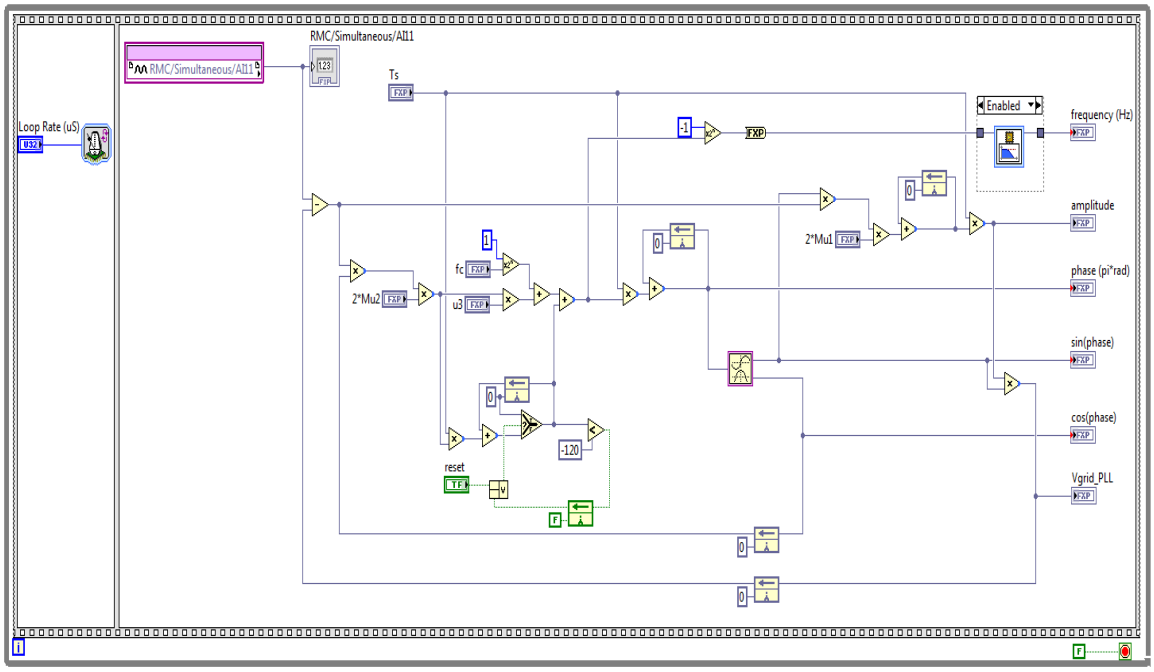


Figure 9.7: Picture of the LabVIEW VI sensing output voltage, v_o using Phase Locked Loop

The output of the Phase Locked Loop is the amplitude of the output voltage signal, v_o. It is then multiplied by an appropriate gain and then compared with the reference output voltage, v_{oref} to determine the error. This error is then passed to the designed feedback compensator to achieve closed loop operation of the converter. A picture of the implementation of the feedback controller in the LabVIEW VI has been displayed in figure 9.8.

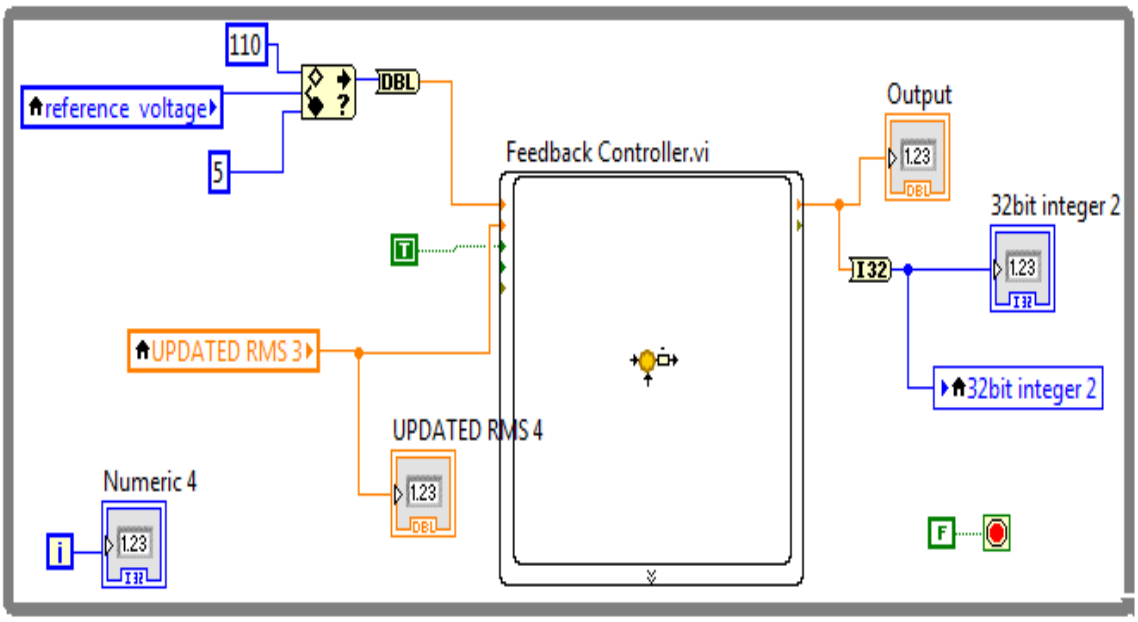


Figure 9.8: Picture of the LabVIEW VI implementing the feedback controller

The experiments results, which have been analyzed in the following sections, are generated using Tektronix MSO-3014 Oscilloscope.

9.3. Operational Experimental Results

The modulation strategy of the converter may be seen from Table 1. The operational experimental results have been shown for v_{oref} = 0.3v_{in} and v_{oref} = 0.8v_{in}. As may be observed from figure 9.9, when desired output peak voltage is less than 0.5v_{in}, the converter switches between 0 and v_{in}/2 sinusoidal waveform. Alternatively, it may be seen in figure 9.10 that, when desired output peak voltage is more than 0.5v_{in}, the converter switches between v_{in}/2 and v_{in} sinusoidal waveforms. It may be seen from figures 9.9 and 9.10, that the output voltage waveforms have high frequency switching harmonics in them.

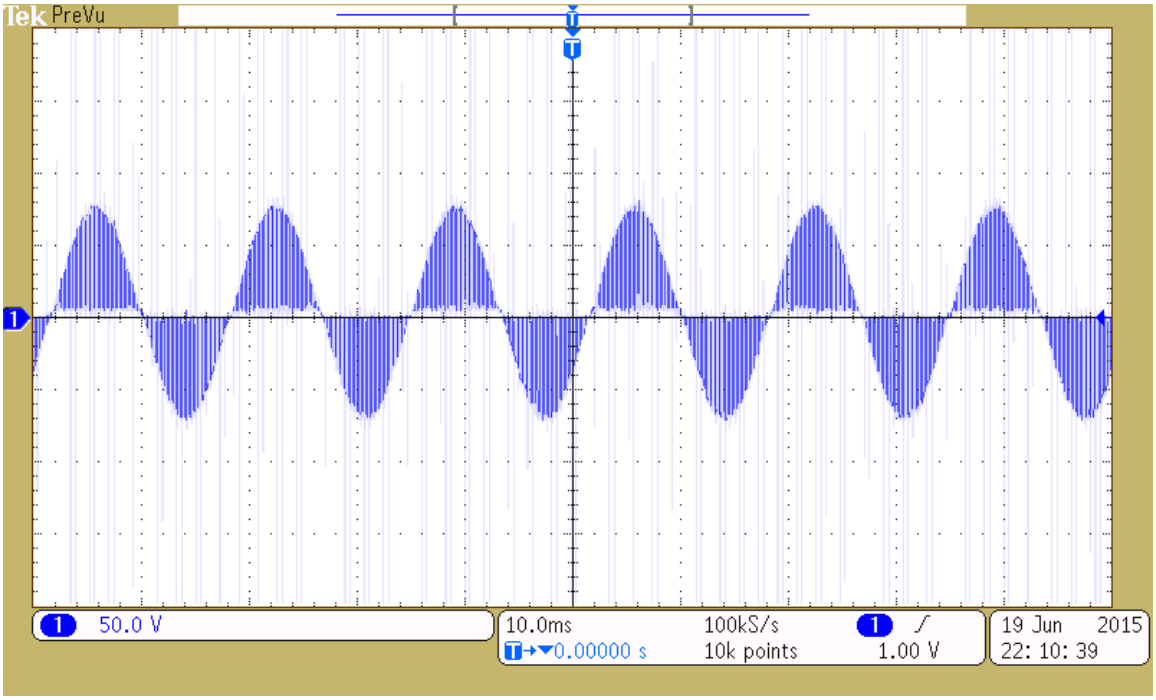


Figure 9.9: Unfiltered Output Voltage waveforms when v_{oref} = 0.3v_{in}

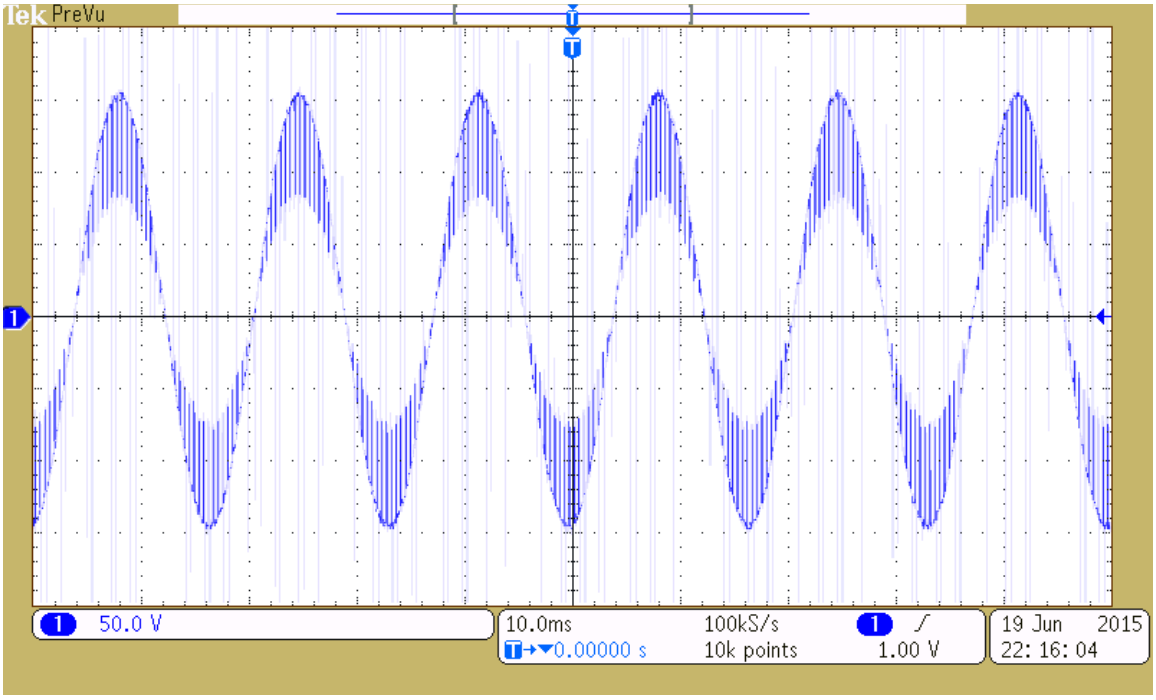


Figure 9.10: Unfiltered Output Voltage waveforms when v_{oref} = 0.8v_{in}

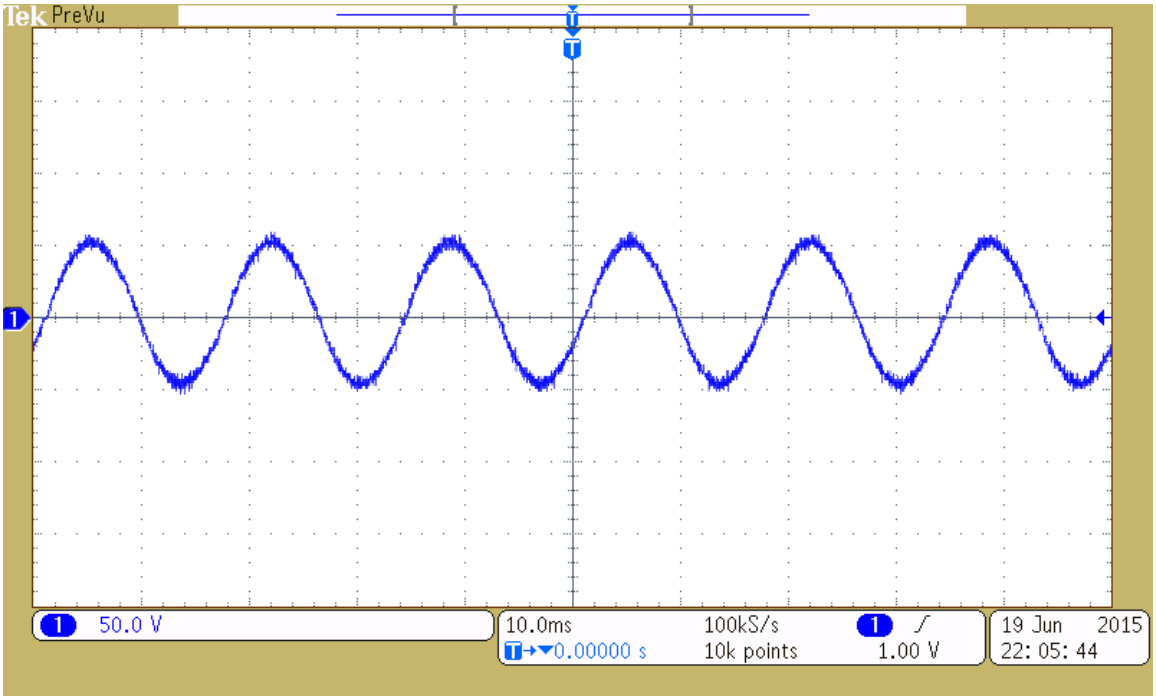


Figure 9.11: Filtered Output Voltage waveforms when v_{oref} = 0.3v_{in}

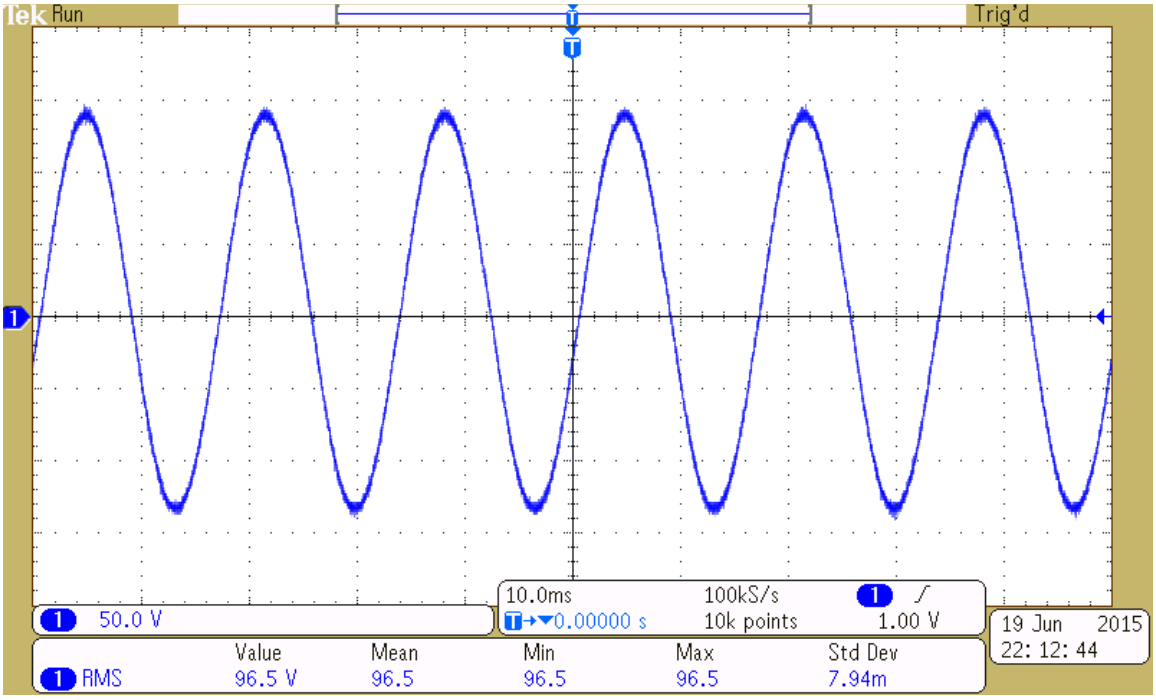


Figure 9.12: Filtered Output Voltage waveforms when v_{oref} = 0.8v_{in}

It may be observed from figures 9.11 and 9.12 that the high frequency switching harmonics seen in figures 9.9 and 9.10 have been attenuated by the introduction of low pass output filter. These waveforms verify the efficacy of the designed output filter. Furthermore, it may also be seen from figures 9.13 and 9.14 that under all conditions, voltages across all switches are clamped to $v_{in}/2$ with the proposed topology. This verifies the practical realization of the concept of Center-Point-Clamping of input source voltage using the technique of input side capacitor voltage balancing as discussed in Section 3.4. Thus, it may be stated that switches rated at half the input voltage can be used to implement the center-point-clamped ac-ac buck converter, thereby increasing the efficacy of the converter as compared to other prevalent ac-ac converter topologies which require switches rated at the input voltage.

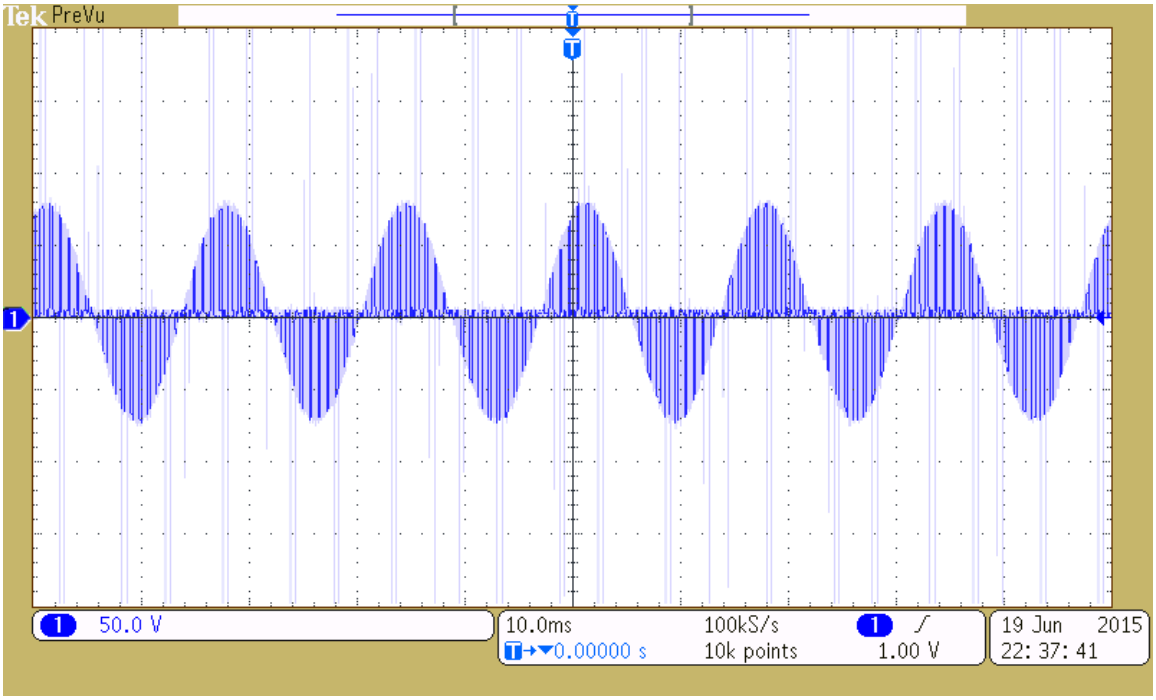


Figure 9.13: Voltages across S2 and S3

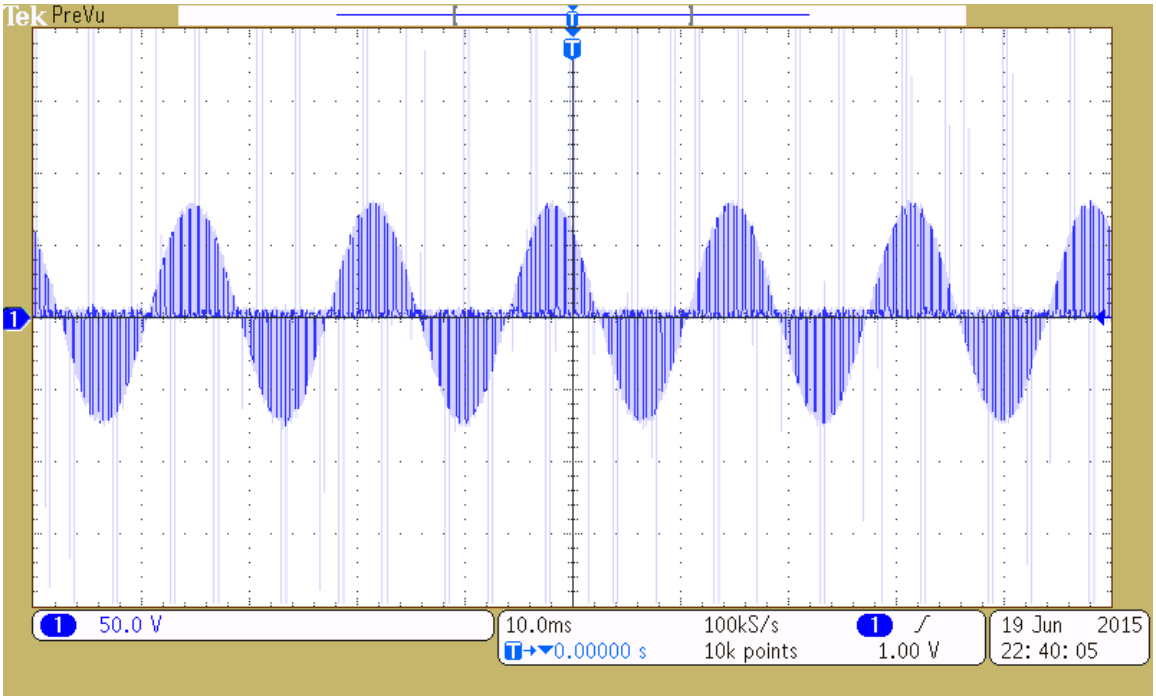


Figure 9.14: Voltages across S_1 and S_4

9.4. Open Loop Experimental Results

The open loop experimental results comprise of the oscilloscope screenshots that have been obtained before the introduction of the feedback controller. These experimental results have been examined in this section. It may be seen from figures 8.9 and 8.10 that the filtered output voltage and current have negligible higher switching harmonics.

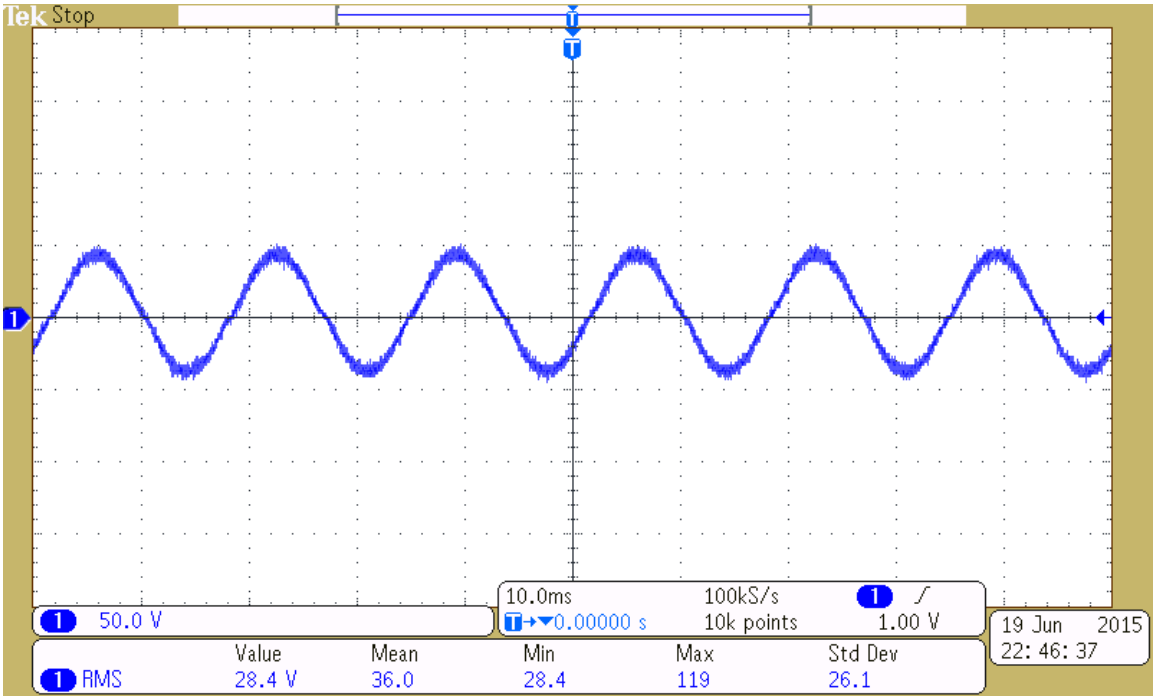


Figure 9.15: Filtered output voltage waveform for D=0.25

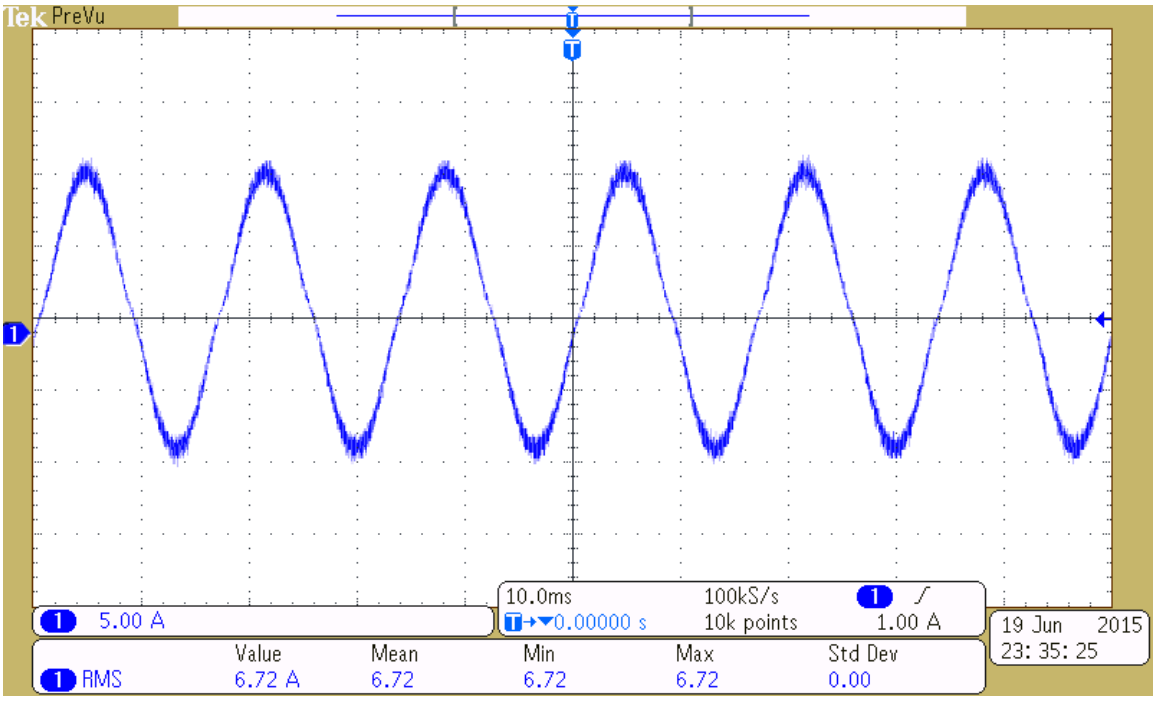


Figure 9.16: Filtered output current waveform for D=0.25

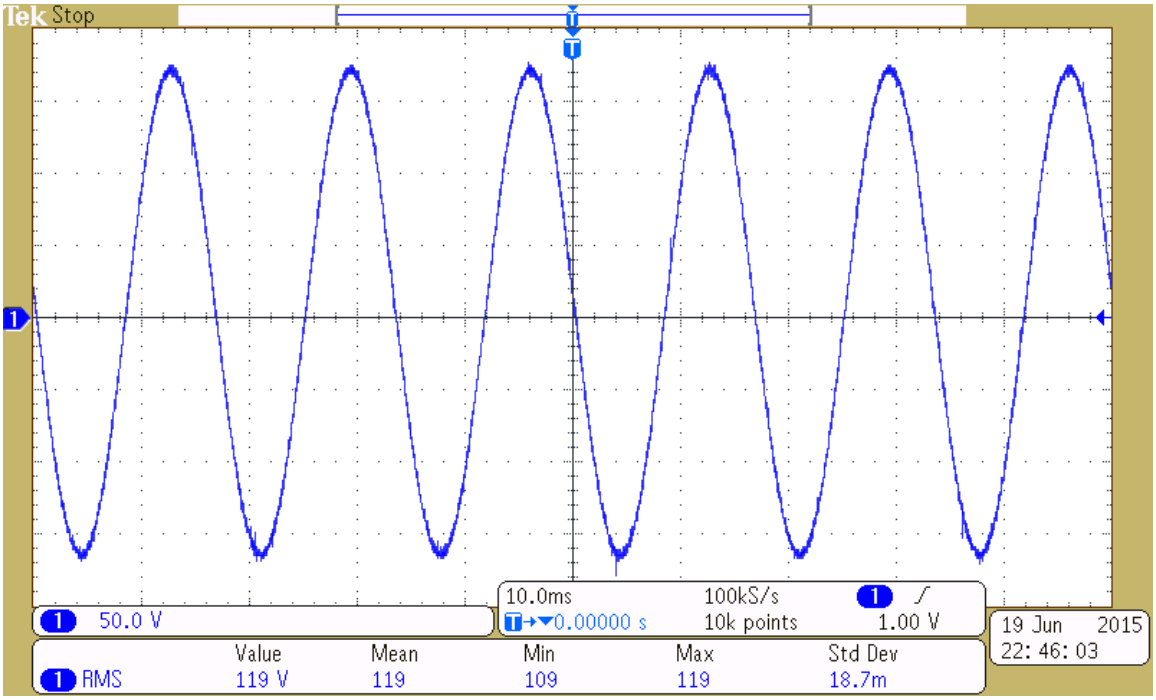


Figure 9.17: Input source voltage waveform for D=0.25

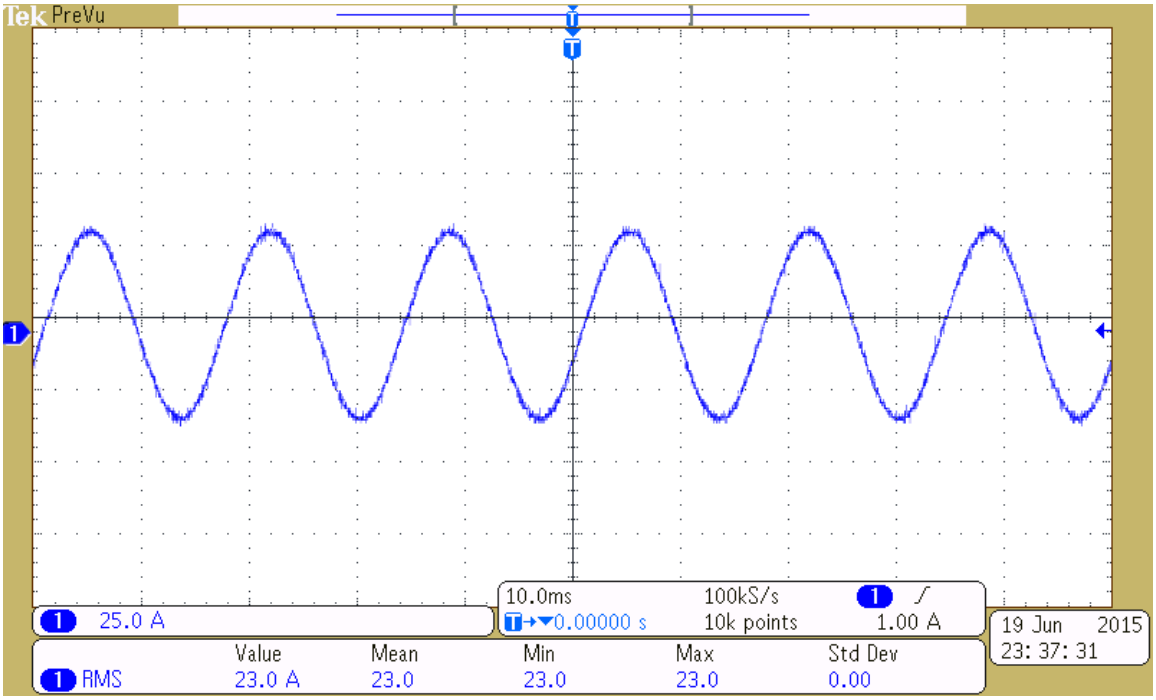


Figure 9.18: Waveform of input current drawn from the source for D=0.25

It may be seen from figures 9.17 and 9.18 that the designed input filter has removed the higher frequency current harmonics from being introduced into the unregulated power supply.

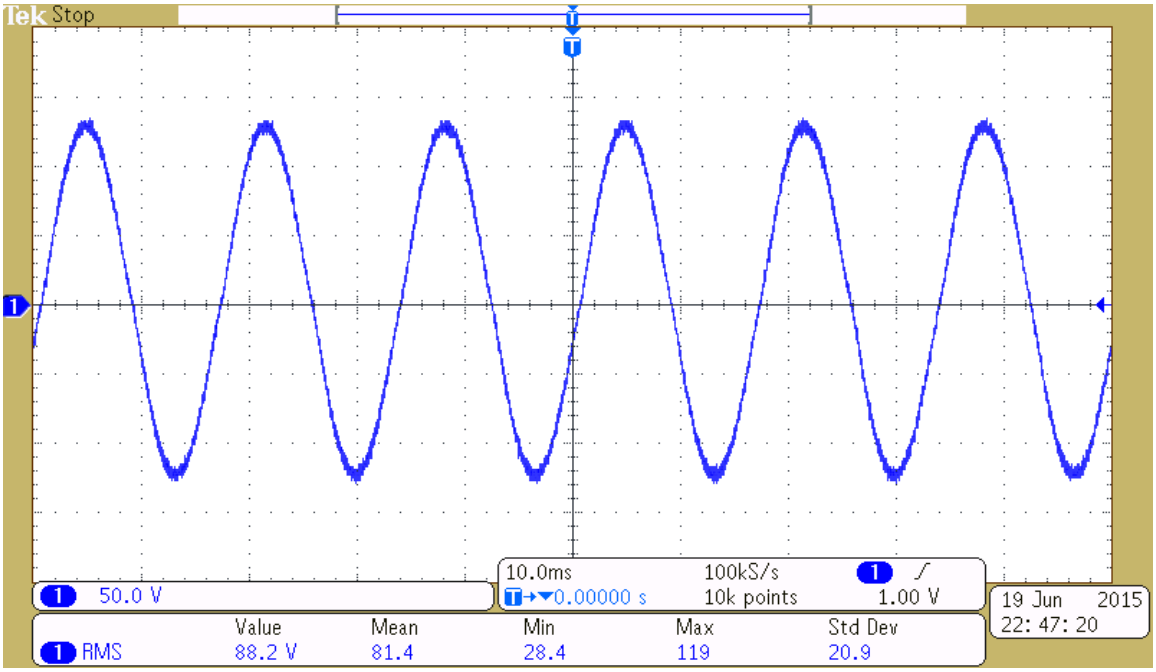


Figure 9.19: Filtered output voltage waveform for D=0.75

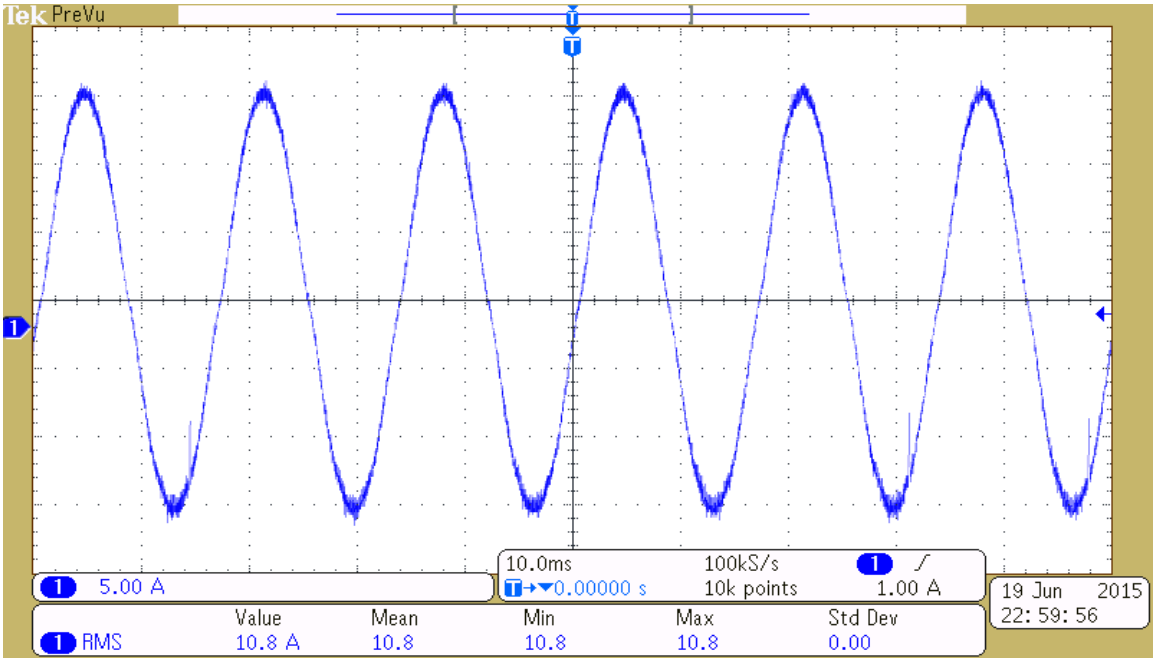


Figure 9.20: Filtered output current waveform for D=0.75

Experimental results shown in figures 9.19 and 9.20 verify the efficacy of the designed output filter in Region 2 ($v_{in}\ to\ v_{in}/2$) of converter operation.

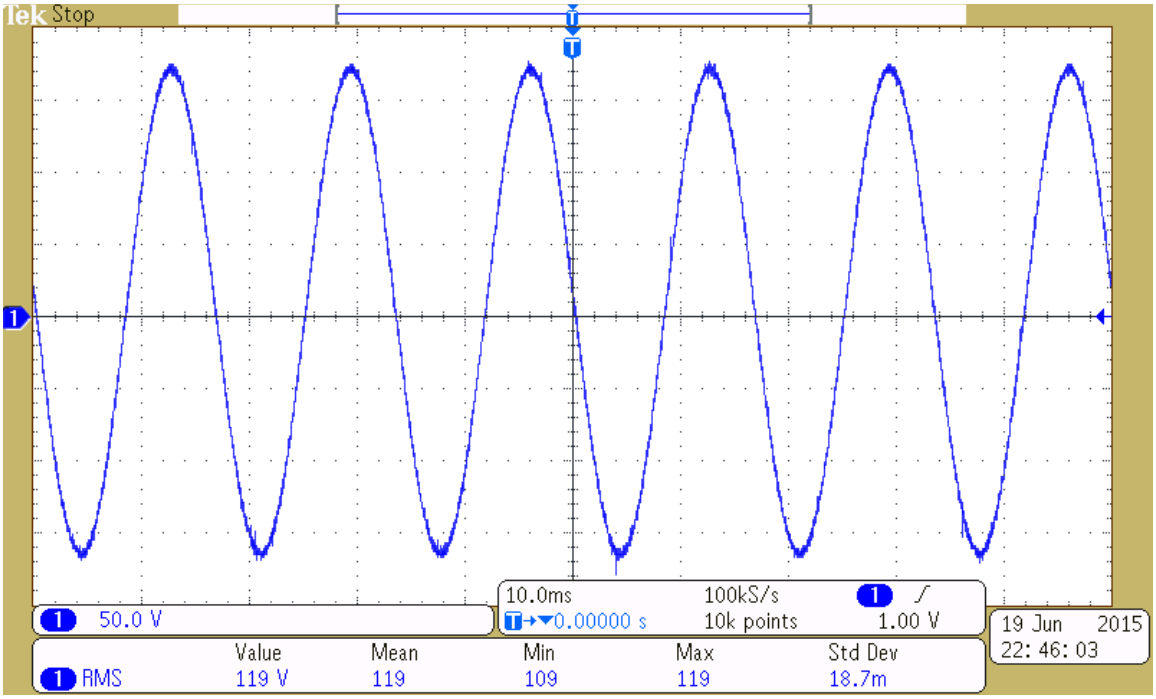


Figure 9.21: Input source voltage waveform for D=0.75

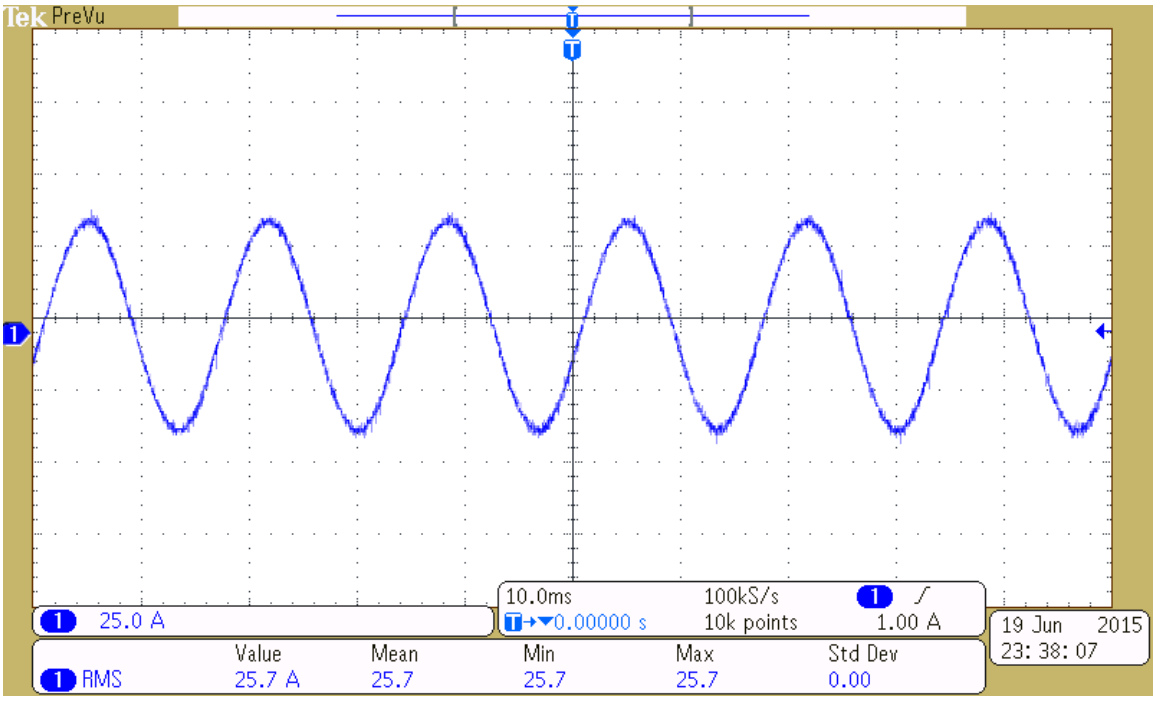


Figure 9.22: Waveform of input current drawn from the source for D=0.75

Experimental results shown in figures 9.21 and 9.22 demonstrate the effectiveness of input filter in eliminating the unwanted higher order frequency harmonics from being fed into the unregulated power supply in case of Region 2 ($v_{in}\ to\ v_{in}/2$) of converter operation.

9.5. Closed Loop Experimental Results

The dynamics associated with the feedback control have been analyzed in this section through the waveforms obtained after introduction of the feedback controller. To illustrate the robustness of the feedback controller, the waveforms pertaining to change of operating point in different regions of converter operation has been discussed here. At first, the operating point is set at v_{oref} = 20V and then suddenly the operating point is changed to 50V within Region 1 (0 to $V_{in}/2$). The response of the feedback controller to this sudden change in operating point may be seen in figure 9.23.

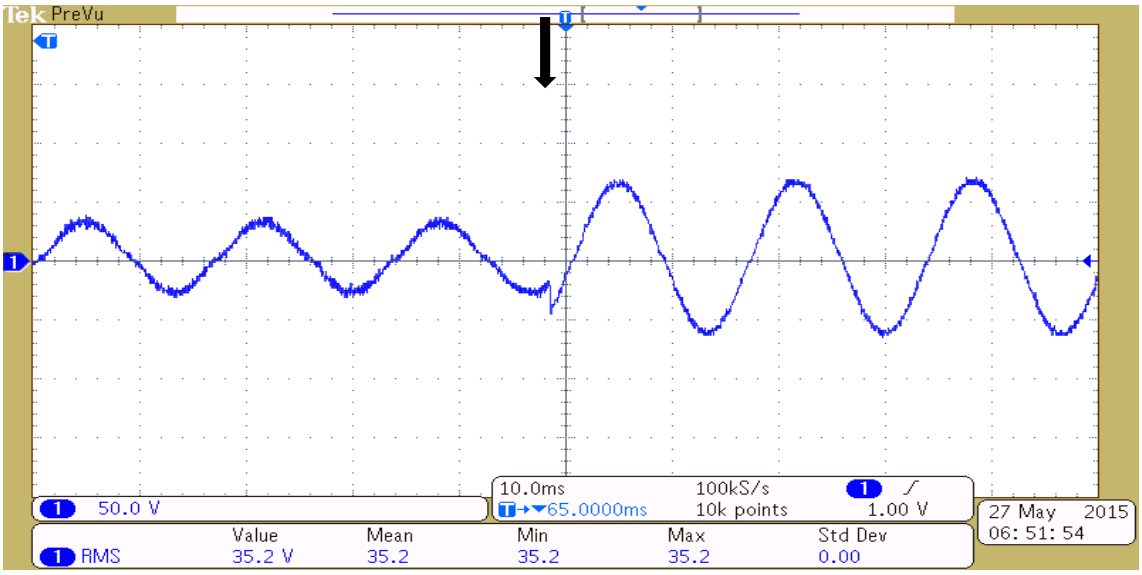


Figure 9.23: Change of operating point within Region 1 (20V to 50V).

In Region 2, initially the operating point is set at v_{oref} = 70V. After system reaches 70V, the operating point is moved within same Region 2 to 90V. This is shown in figure 9.24.

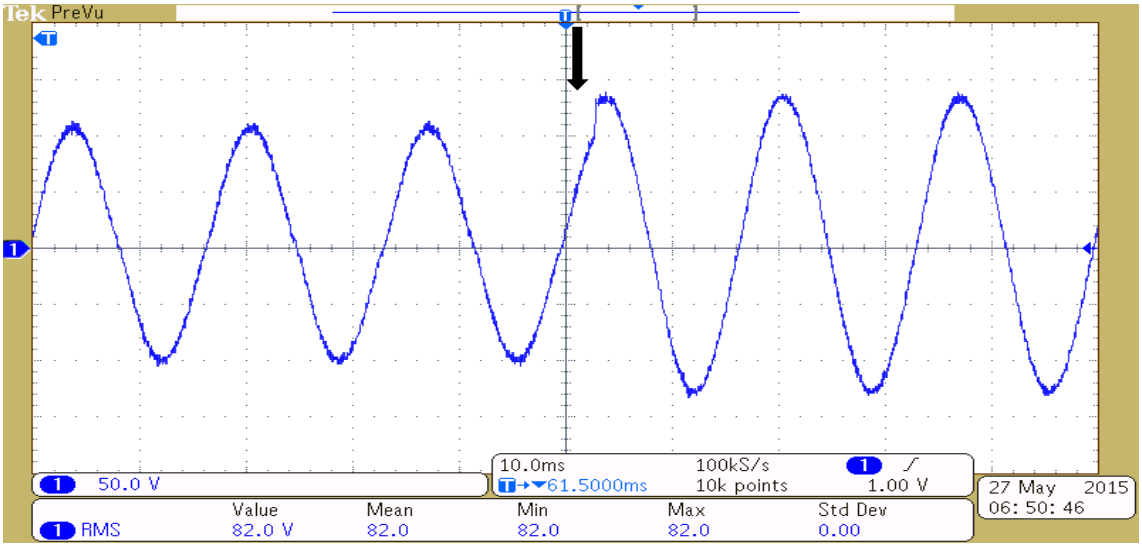


Figure 9.24: Change of operating point within Region 2 (70V to 90V).

Finally, in Region 1, initially operating point is set at v_{oref}= 20V. After system reaches 20V, operating point is moved to Region 2 to 90V. This is shown in figure 9.25.

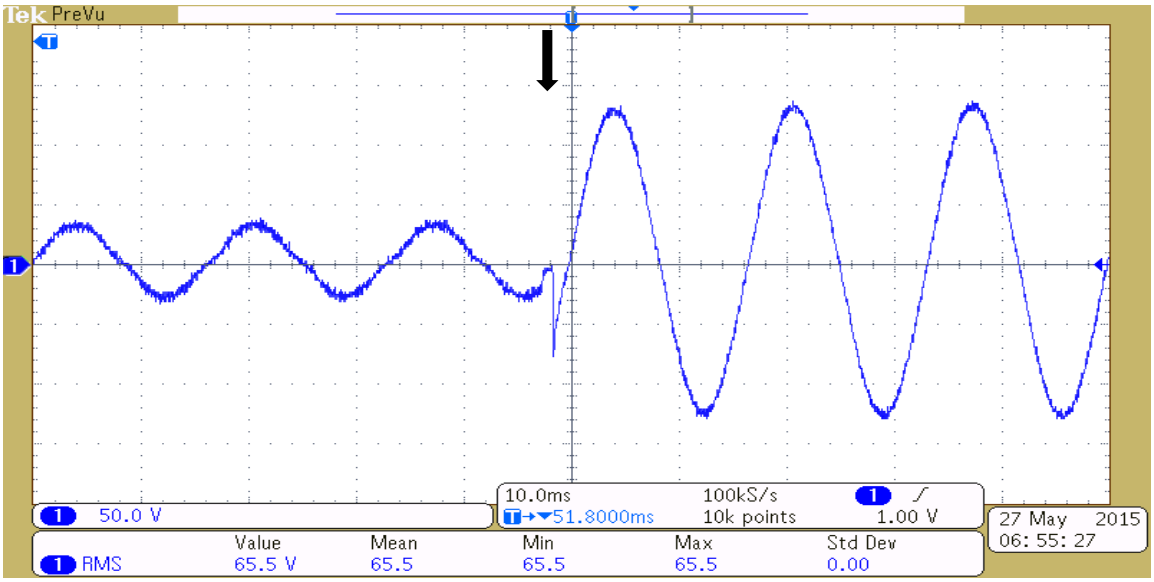


Figure 9.25: Change of operating point from Region 1 (20V) to Region 2 (90V).

It may be seen from figures 9.23, 9.24, and 9.25, that upon change of operating point, the output voltage exhibits a sub-cycle transient and then settles to the desired operating point in one-two fundamental cycles. This verifies the efficacy of the command following performance of the feedback compensator.

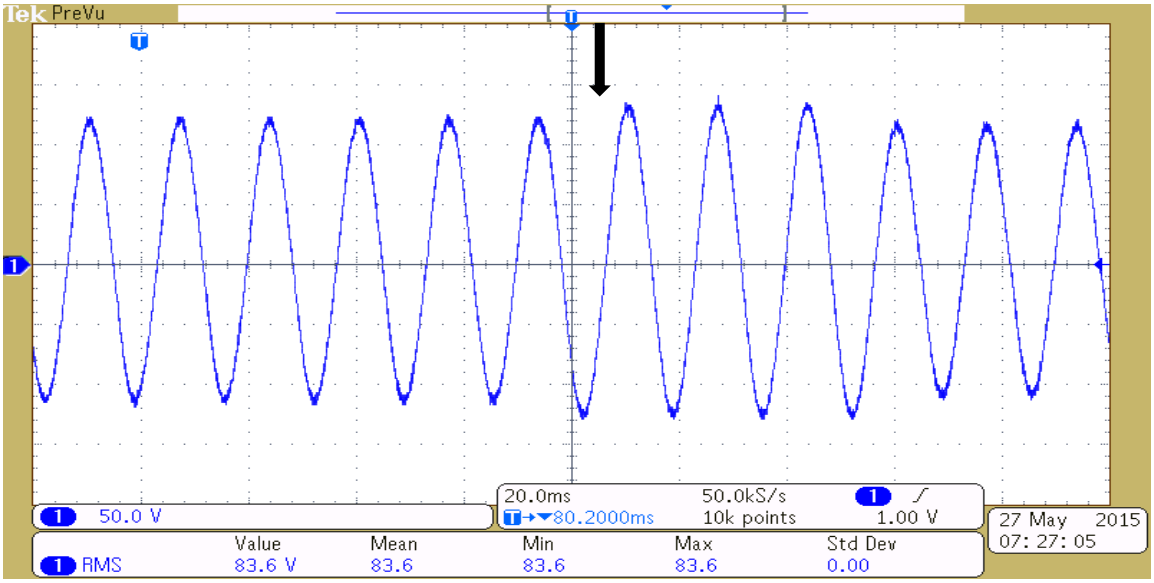


Figure 9.26: Line regulation: performance during step increase in line voltage when v_{oref}= 80V.

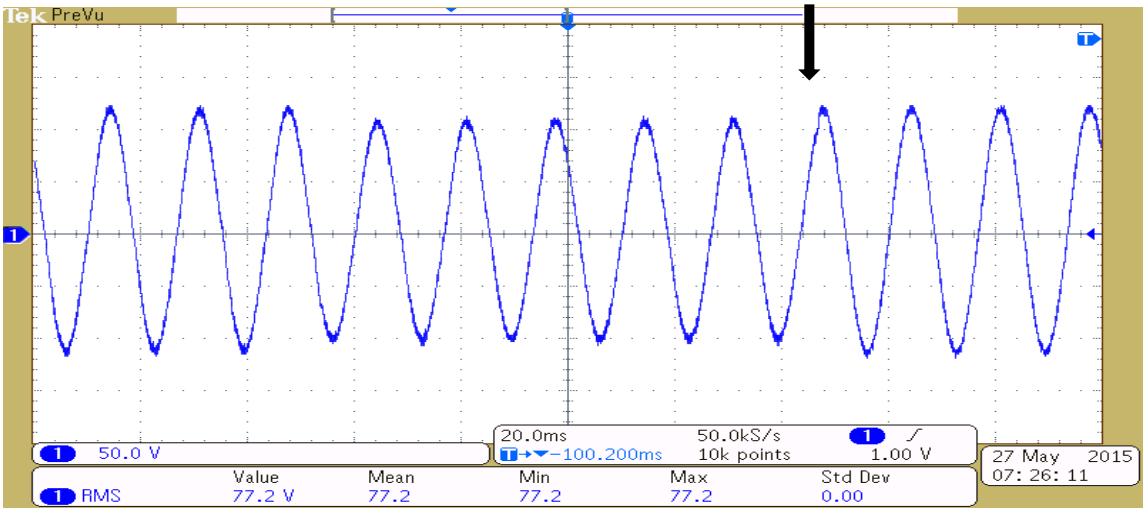


Figure 9.27: Line regulation: performance during step decrease in line voltage when v_{oref}= 80V.

To evaluate the line regulation performance of center-point-clamped ac-ac converter under varying source voltages, input voltage is varied by +10% and –10% of 120Vac. First, this ac voltage is increased by 10%, and its effect on the output voltage waveform is shown in figure 9.26. Next, the line voltage is decreased by 10%, and its effect on the output voltage waveform is shown in figure 9.27.

As may be seen from figure 9.26, when the line voltage experiences a spike of 10%, the output voltage exhibits a minimal change. Similarly, as illustrated in figure 9.27, when the line voltage experiences sag of 10%, the output voltage exhibits a negligible effect. This illustrates the command following performance of the system.

Finally, to evaluate the load regulation performance of center-point-clamped ac-ac buck converter under varying load currents, load current is decreased, and its effect on the output voltage waveform is shown in figure 9.28.

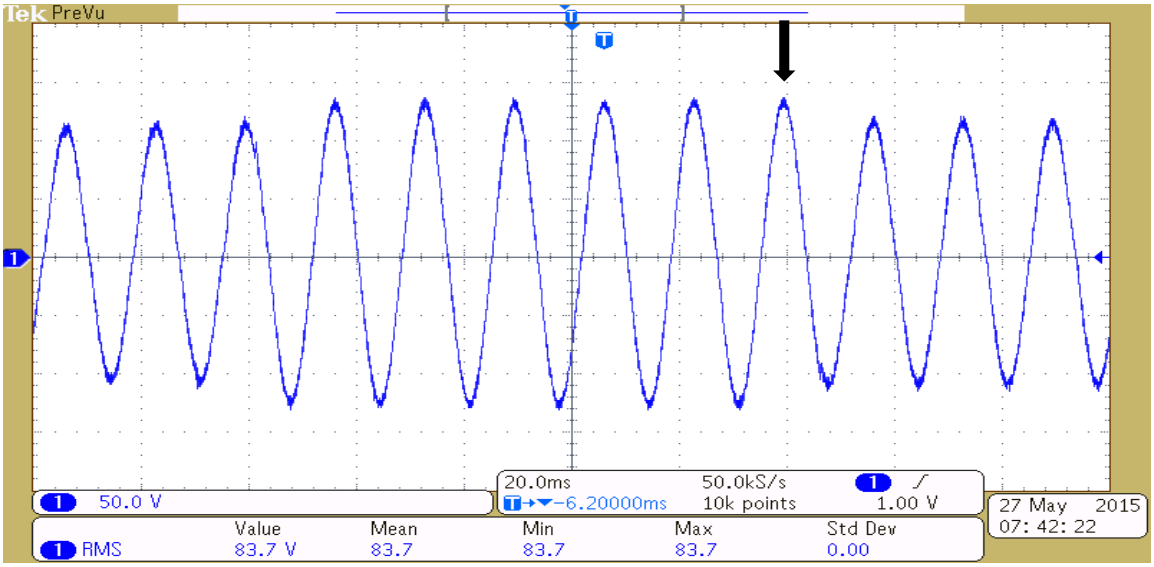


Figure 9.28: Load regulation: performance during step decrease in load current when v_{oref}= 80V.

Next, load current is increased, and its effect on the output voltage waveform is shown in figure 9.29.

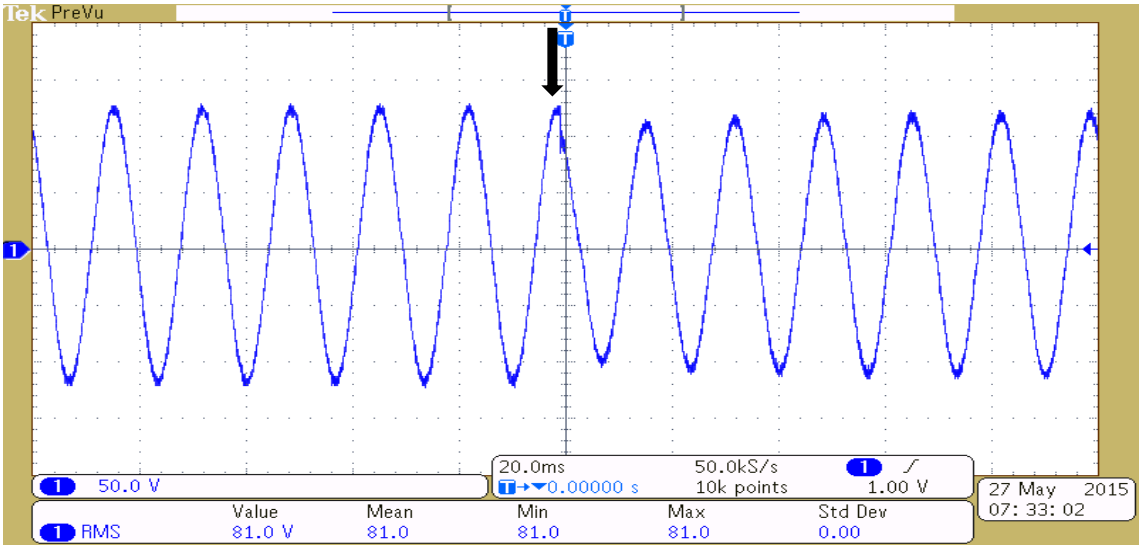


Figure 9.29: Load regulation: performance during step increase in load current when v_{oref}= 80V.

As may be seen from figure 9.28, when the load drops, the output voltage exhibits a small overshoot and then decreases to the original value in two-three fundamental cycles. Similarly, when the load suddenly increases, the output voltage exhibits a small undershoot and then increases to the original value in two-three fundamental cycles. This is illustrated in figure 9.29.

CHAPTER 10 : FAMILY OF CENTER-POINT-CLAMPED AC-AC CONVERTERS

10.1. Introduction

This chapter discusses the family of direct ac-ac power converters, which has been aptly termed as family of Center-Point-Clamped Direct AC-AC Power Converters. This family of converters involves Center-Point-Clamped Direct AC-AC Buck Converter, Center-Point-Clamped Direct AC-AC Boost Converter, Center-Point-Clamped Direct AC-AC Buck-Boost Converter, and Center-Point-Clamped Direct AC-AC Ćuk Converter. The main objective behind this novel family of converters is the use of these converter topologies to improve the efficiency of power electronic based power quality improving devices. The efficiency of these power quality devices are improved on employment of these novel topologies as this family of converters employ semiconductor devices rated at half the rating of semiconductor devices employed to build other popular converter topologies. The operating principles as well as the switching sequence of these novel converters have been discussed in the following sections. Simulation results verifying the operation methodologies of these converters have also been presented in the following sections.

10.2. Center-Point-Clamped Direct AC-AC Buck Converter

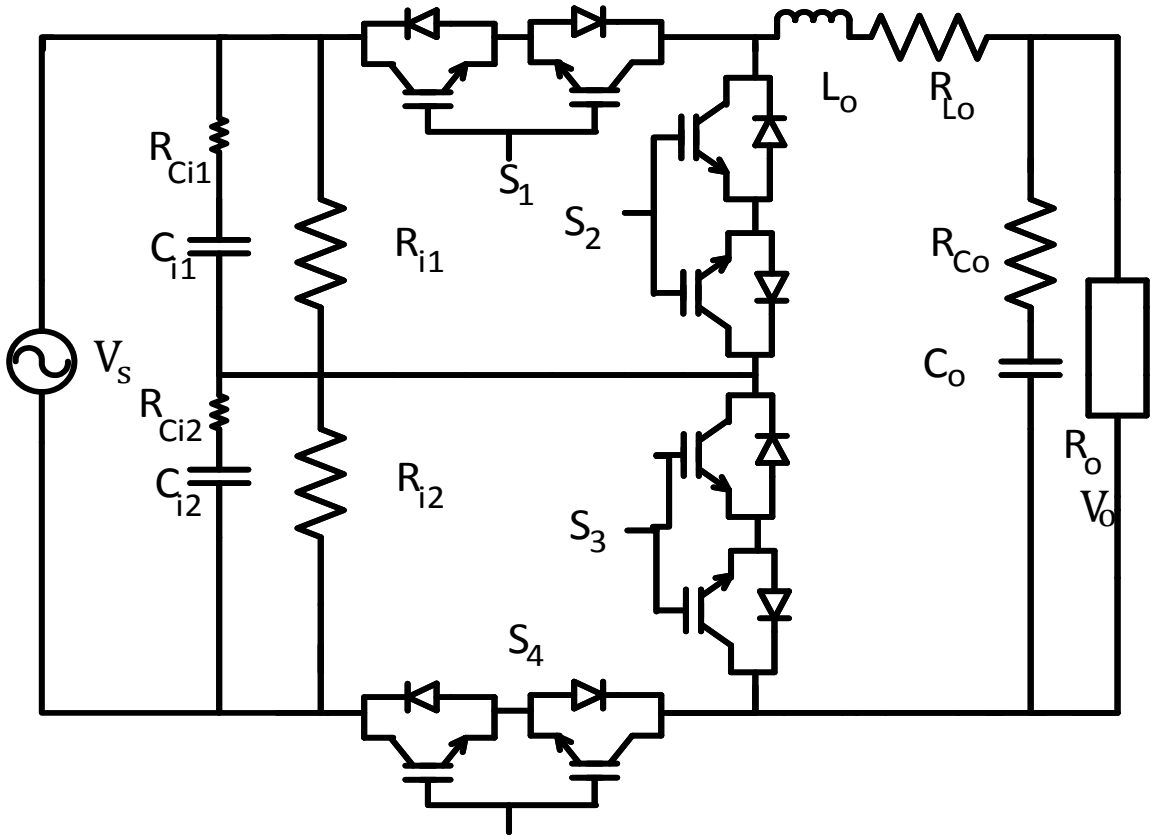


Figure 10.1: Simplified Circuit Schematic of a Center-Point-Clamped Direct AC-AC Buck Converter

Figure 10.1 shows the simplified circuit schematic of the Center-Point-Clamped Direct AC-AC Buck Converter that belongs to the novel family of Center-Point-Clamped Direct AC-AC Power Converters. This converter topology has been discussed in detail in this thesis. The switching sequence has been described again in Table 5.

Table 5: Switching Pattern of the Center-Point-Clamped Direct AC-AC Buck Converter

Command v_{oref} (desired output)	between 0 and $v_{in}/2$	between $v_{in}/2$ and v_{in}
State 1	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 2	S_2 S_4 closed S_1 S_3 open	S_2 S_4 closed S_1 S_3 open
State 3	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 4	S_1 S_3 closed S_2 S_4 open	S_1 S_3 closed S_2 S_4 open

The operating principle of the converter topology has been analyzed elaborately in this thesis. Simulation results as well as experimental results verifying the working principle of this converter topology has been presented in this thesis. The simulation results verifying the two regions of converter operation has been shown in figure 10.2 and figure 10.3.

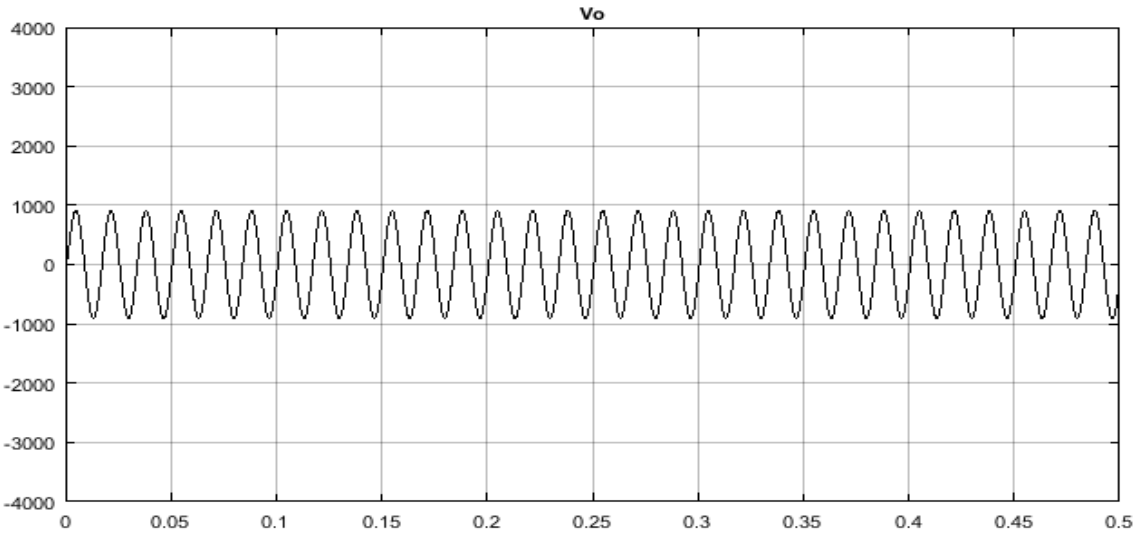


Figure 10.2: Filtered output voltage waveform for D=0.25

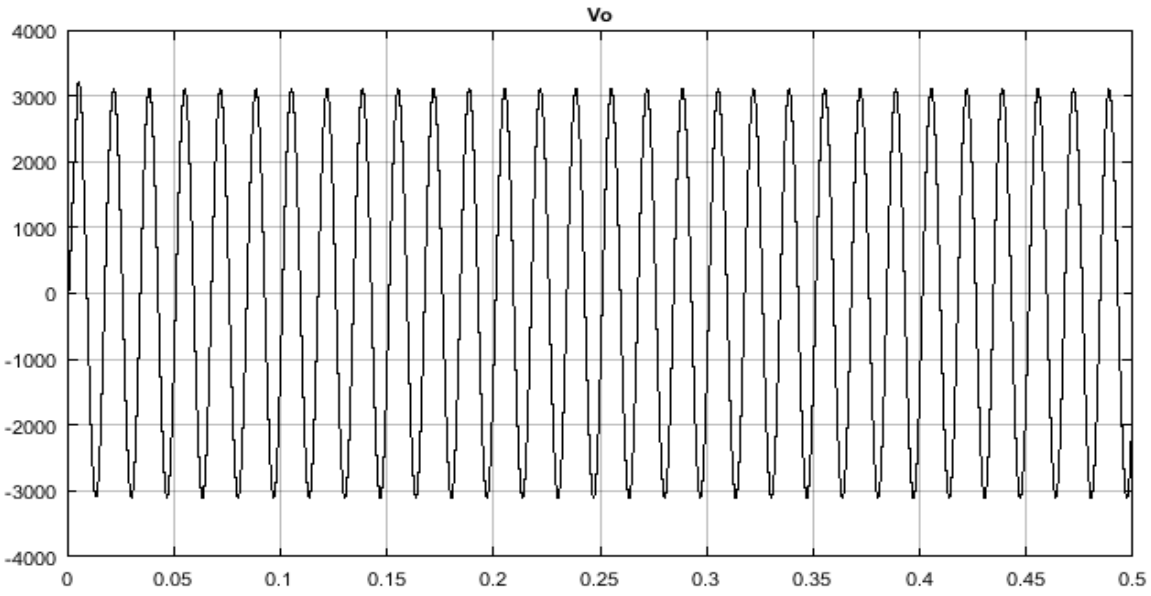


Figure 10.3: Filtered output voltage waveform for D=0.75

The popular direct ac-ac buck converter topologies employ semiconductor devices rated at the source voltage but the center-point-clamped direct ac-ac buck converter employs semiconductor switches rated at half the magnitude of converter input voltage. Thus, it may be concluded that the employment of lower voltage rated power semiconductor devices increases the power efficiency of the center-point-clamped direct ac-ac buck converter topology as compared to other popular buck converter topologies. This verifies the efficacy of the novel topology of center-point-clamped ac-ac buck converter.

10.3. Center-Point-Clamped Direct AC-AC Boost Converter

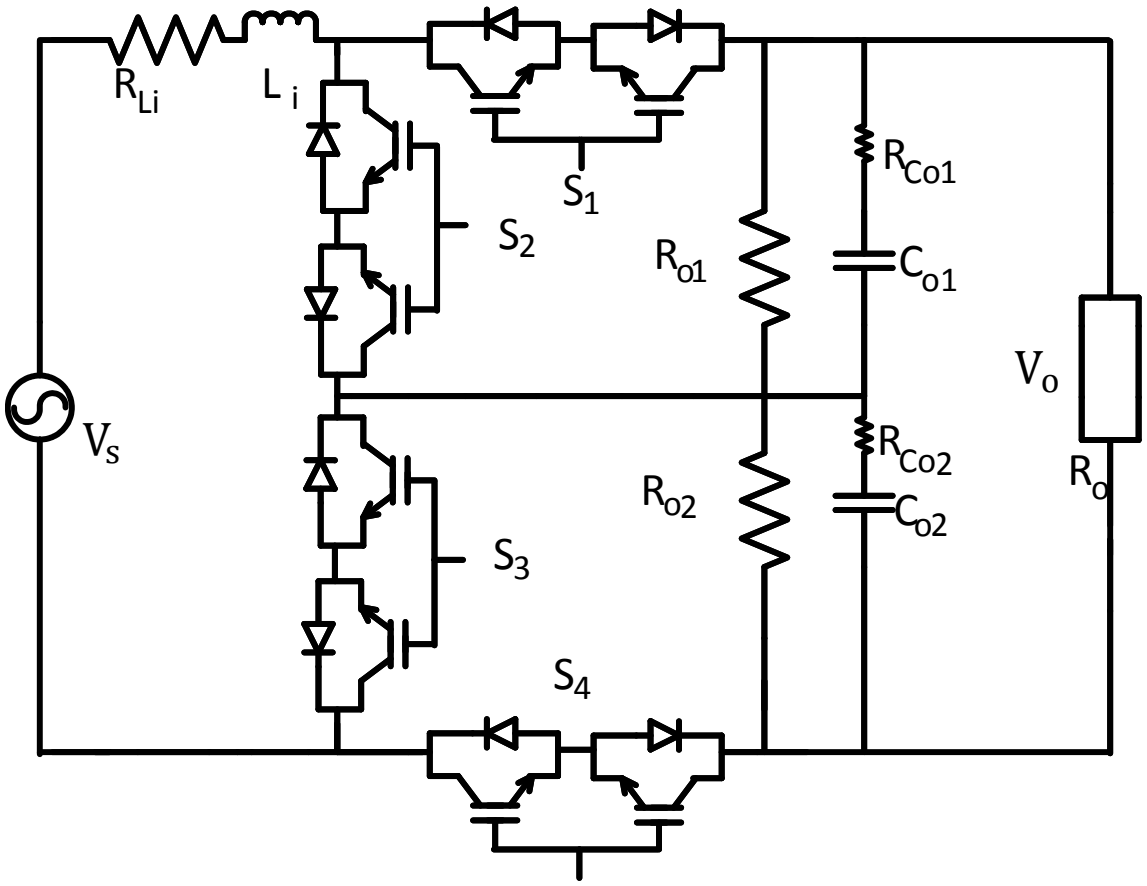


Figure 10.4: Simplified Circuit Schematic of a Center-Point-Clamped Direct AC-AC Boost Converter

Figure 10.4 shows the simplified circuit schematic of the Center-Point-Clamped Direct AC-AC Boost Converter that belongs to the novel family of Center-Point-Clamped Direct AC-AC Power Converters. The switching sequence of this novel converter topology has been shown in Table 6.

Table 6: Switching Pattern of the Center-Point-Clamped Direct AC-AC Boost Converter

Command v_{oref} (desired output)	between 0 and Mv_{in}
State 1	S_1 S_4 closed S_2 S_3 open
State 2	S_1 S_4 open S_2 S_3 closed

It may be seen in Table 6 that when the bidirectional switches S_1 and S_4 are closed and the bidirectional switches S_2 and S_3 are open, the converter output voltage, v_o is zero. But when the bidirectional switches S_1 and S_4 are open and the bidirectional switches S_2 and S_3 are closed, the converter output voltage, v_o is Mv_{in}, where M represents the voltage conversion ratio of this converter topology, which is as follows:

$M = 1/(1-D)$, where D is the duty ratio of this converter topology.

Here, $D = t_{on}/(t_{on}+t_{off})$, where t_{on} is the time duration during which the bidirectional switch is closed and t_{off} is the time duration during which the bidirectional switch is open.

The main objective behind this novel topology of Center-Point-Clamped Direct AC-AC Boost Converter is to reduce the voltage stress across the bidirectional switches of the converter. It may be observed that conventional AC-AC Boost Converter topologies require semiconductor devices rated at desired output voltage, i.e. v_o. But this novel converter topology employs semiconductor devices rated at half the voltage ratings as that of the conventional converter topologies, $v_o/2$.

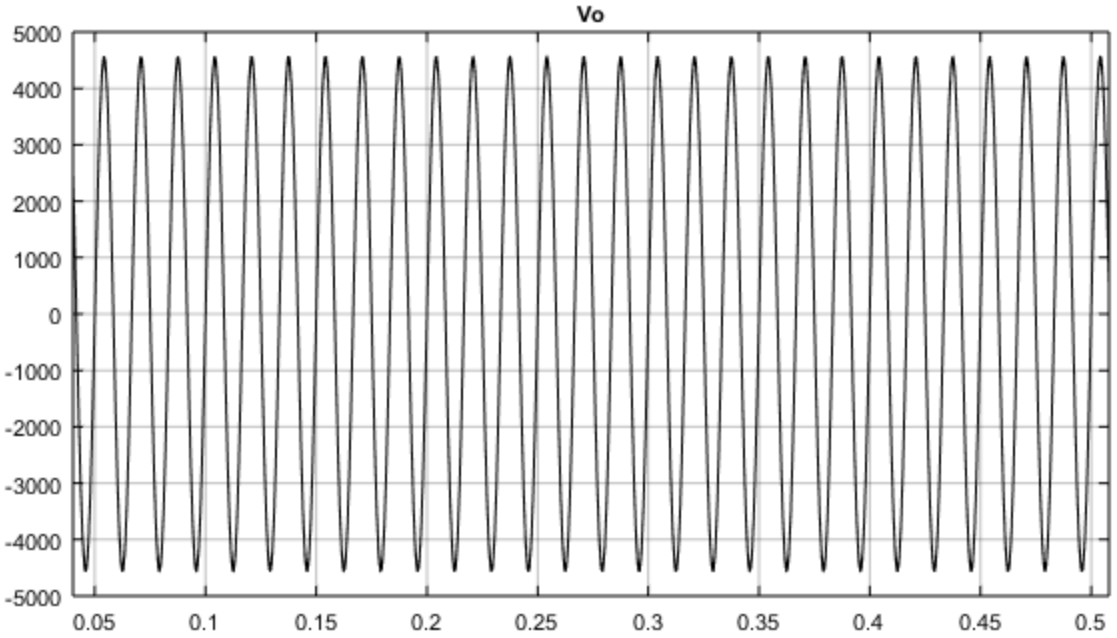


Figure 10.5: Filtered output voltage waveform for D=0.25

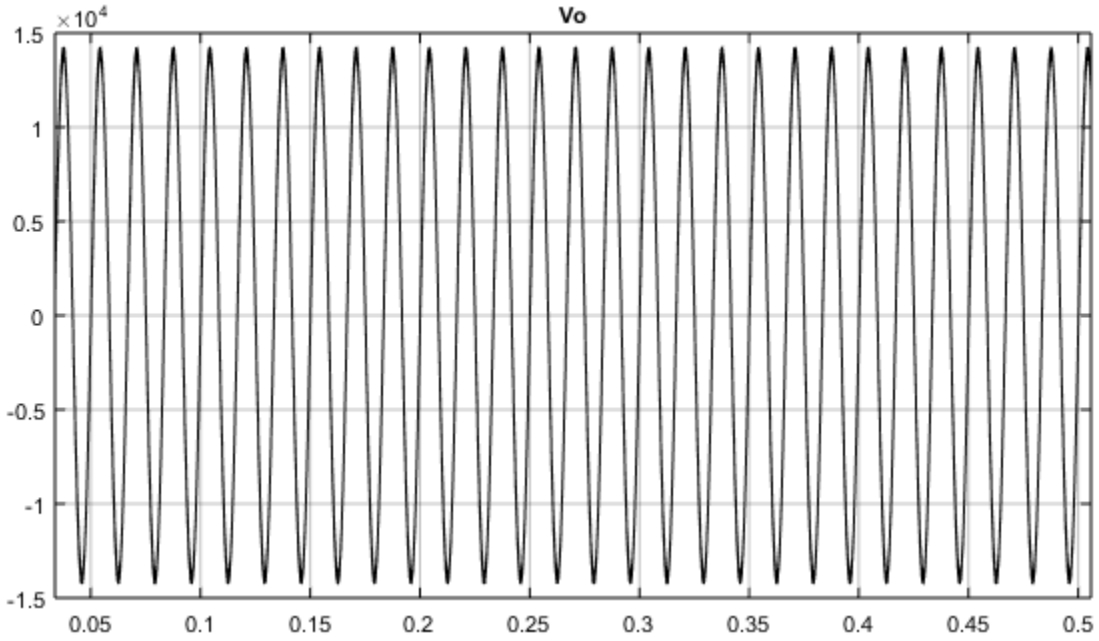


Figure 10.6: Filtered output voltage waveform for D=0.75

Simulation results verifying the operation of the converter for duty ratio of D=0.25 and D=0.75 are presented in figures 10.5 and 10.6. These simulation results prove the efficacy of the Center-Point-Clamped Direct AC-AC Boost Converter.

10.4. Center-Point-Clamped Direct AC-AC Buck-Boost Converter

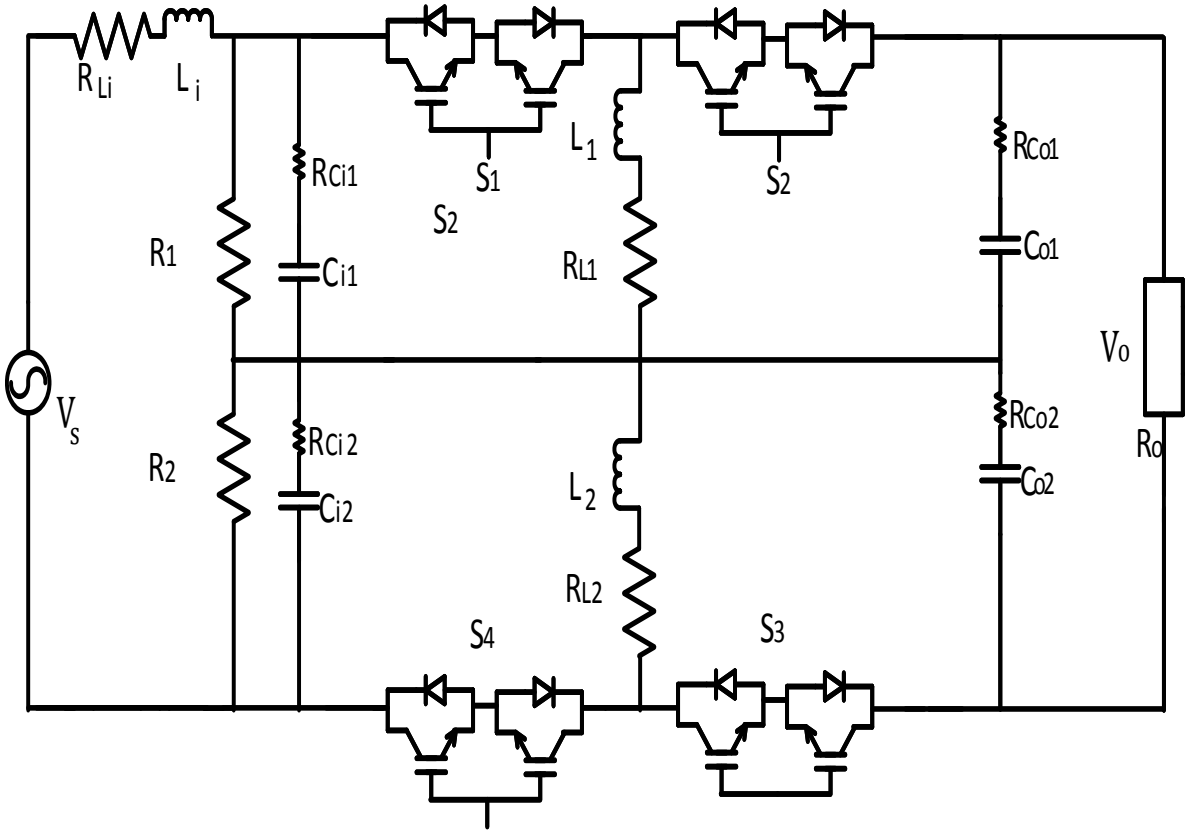


Figure 10.7: Simplified Circuit Schematic of a Center-Point-Clamped Direct AC-AC Buck-Boost Converter

Figure 10.7 shows the simplified circuit schematic of the Center-Point-Clamped Direct AC-AC Buck-Boost Converter that belongs to the family of Center-Point-Clamped Direct AC-AC Power Converters. The switching sequence of this novel converter topology has been shown in Table 7.

Table 7: Switching Pattern of the Center-Point-Clamped Direct AC-AC Buck-Boost Converter

Command v_{oref} (desired output)	between 0 and Mv_{in}
State 1	S_1 S_4 closed S_2 S_3 open
State 2	S_1 S_4 open S_2 S_3 closed

It may be seen in Table 7 that when the bidirectional switches S_1 and S_4 are closed and the bidirectional switches S_2 and S_3 are open, the converter output voltage, v_o is zero. But when the bidirectional switches S_1 and S_4 are open and the bidirectional switches S_2 and S_3 are closed, the converter output voltage, v_o is Mv_{in}, where M represents the voltage conversion ratio of this converter topology, which is as follows:

$M = D/(1\text{-}D)$, where D is the duty ratio of this converter topology.

Here, $D = t_{on}/(t_{on}+t_{off})$, where t_{on} is the time duration during which the bidirectional switch is closed and t_{off} is the time duration during which the bidirectional switch is open.

The main objective behind this novel topology of Center-Point-Clamped Direct AC-AC Buck-Boost Converter is to reduce the voltage stress across the bidirectional switches of the converter. It may be observed that conventional AC-AC Buck-Boost Converter topologies require semiconductor devices rated at summation of the input and desired output voltages, i.e $v_o + v_s$. But this novel converter topology employs semiconductor devices rated at half the voltage ratings as that of the conventional converter topologies, $(v_o + v_s)/2$.

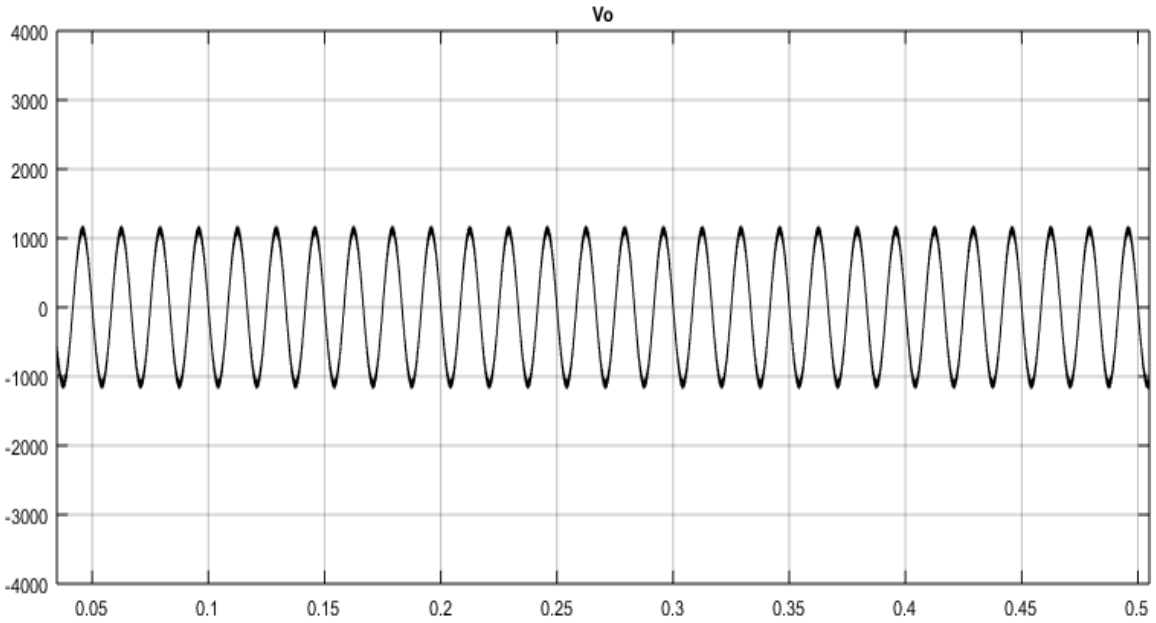


Figure 10.8: Filtered output voltage waveform for D=0.25

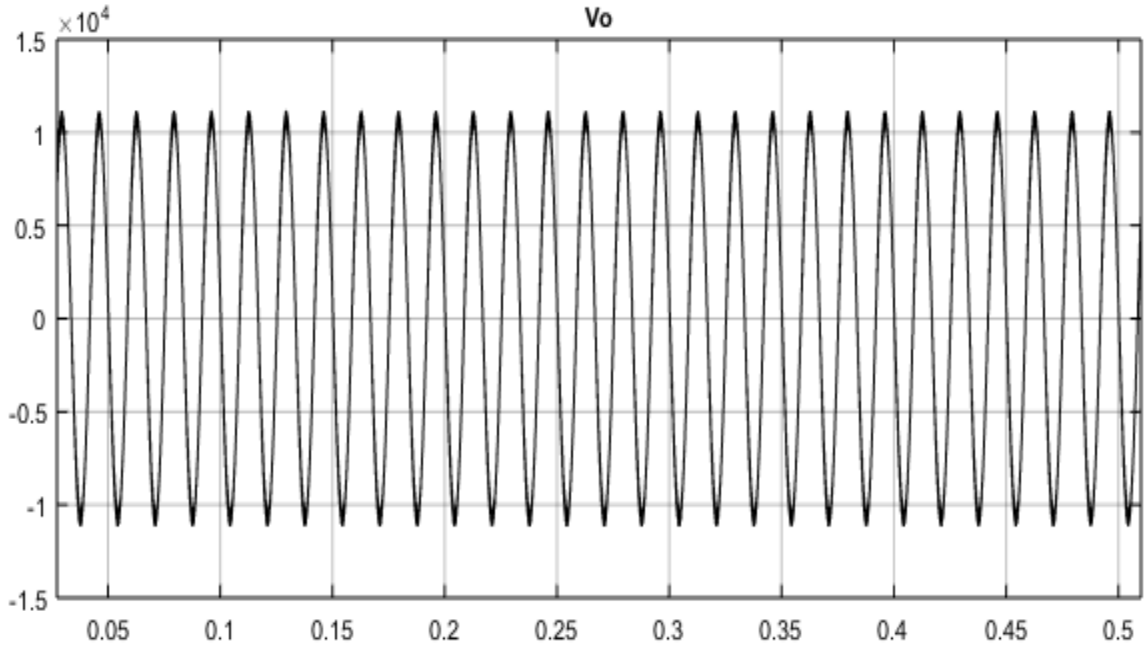


Figure 10.9: Filtered output voltage waveform for D=0.75

Simulation results verifying the operation of the converter for duty ratio of D=0.25 and D=0.75 are presented in figure 10.8 and 10.9. These simulation results verify the

operation methodology as well as efficacy of the Center-Point-Clamped Direct AC-AC Buck-Boost Converter.

10.5. Center-Point-Clamped Direct AC-AC Ćuk Converter

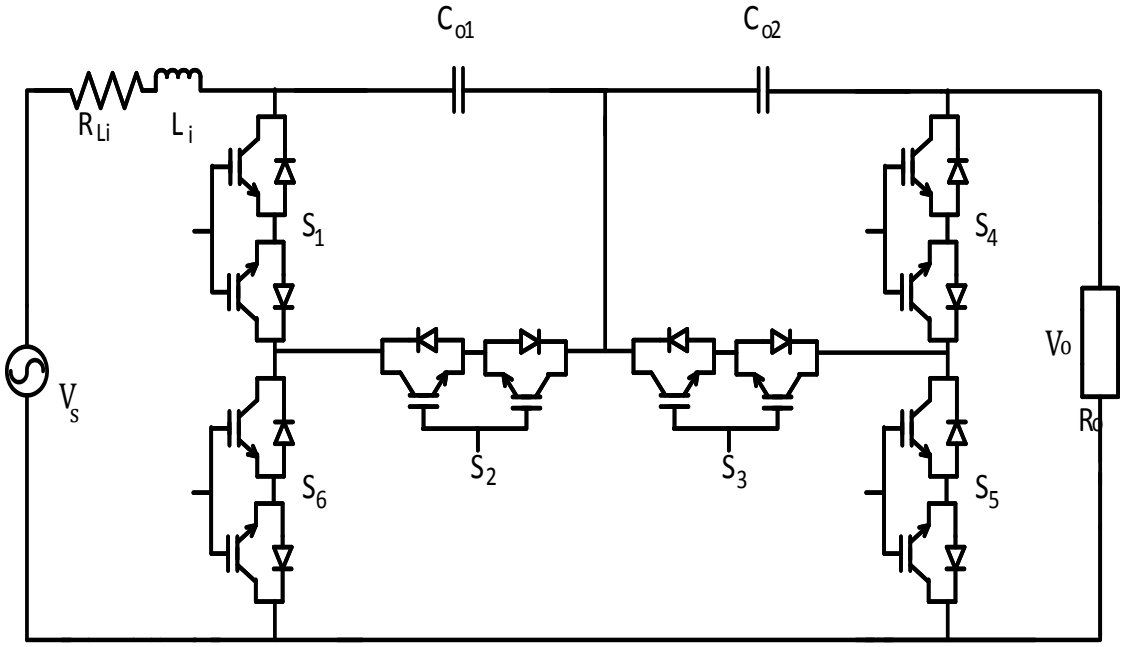


Figure 10.10: Simplified Circuit Schematic of a Center-Point-Clamped Direct AC-AC Ćuk Converter

Figure 10.10 shows the simplified circuit schematic of the Center-Point-Clamped Direct AC-AC Ćuk Converter that belongs to the novel family of Center-Point-Clamped Direct AC-AC Power Converters. The switching sequence of this novel converter topology has been shown in Table 8.

Table 8: Switching Pattern of the Center-Point-Clamped Direct AC-AC Ćuk Converter

Command v_{oref} (desired output)	between 0 and Mv_{in}
State 1	S_1 S_2 S_3 S_6 closed S_4 S_5 open
State 2	S_1 S_6 open S_2 S_3 S_4 S_5 closed

It may be seen in Table 8 that when the bidirectional switches $S_{1,}$ $S_{2,}$ S_3 and S_6 are closed and the bidirectional switches S_4 and S_5 are open, the capacitors, C_{o1} and C_{o2} transfer the energy to the load. But when the bidirectional switches S_1 and S_6 are open and the bidirectional switches $S_{2,}$ $S_{3,}$ S_4 and S_5 are closed, energy is transferred from the input side source to the capacitors, C_{o1} and C_{o2}. Here, M represents voltage conversion ratio of the converter topology, which is as follows:

$M = D/(1\text{-}D)$, where D is the duty ratio of this converter topology.

Here, $D = t_{on}/(t_{on} + t_{off})$, where t_{on} is the time duration during which the bidirectional switch is closed and t_{off} is the time duration during which the bidirectional switch is open.

The main objective behind this novel topology of Center-Point-Clamped Direct AC-AC Ćuk Converter is to reduce the voltage stress across the bidirectional switches of the converter. It may be observed that conventional AC-AC Ćuk Converter topologies require semiconductor devices rated at summation of the input and desired output voltages, i.e. $(v_o + v_s)$. But this novel converter topology employs semiconductor devices rated at half the voltage ratings as that of the conventional converter topologies, $(v_o + v_s)/2$.

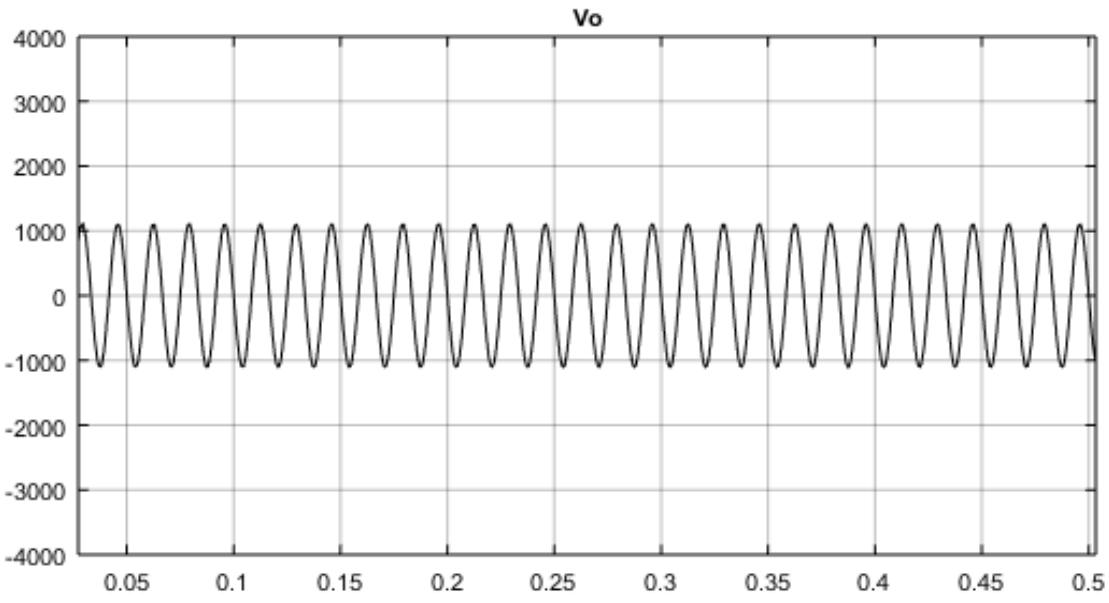


Figure 10.11: Filtered output voltage waveform for D=0.25

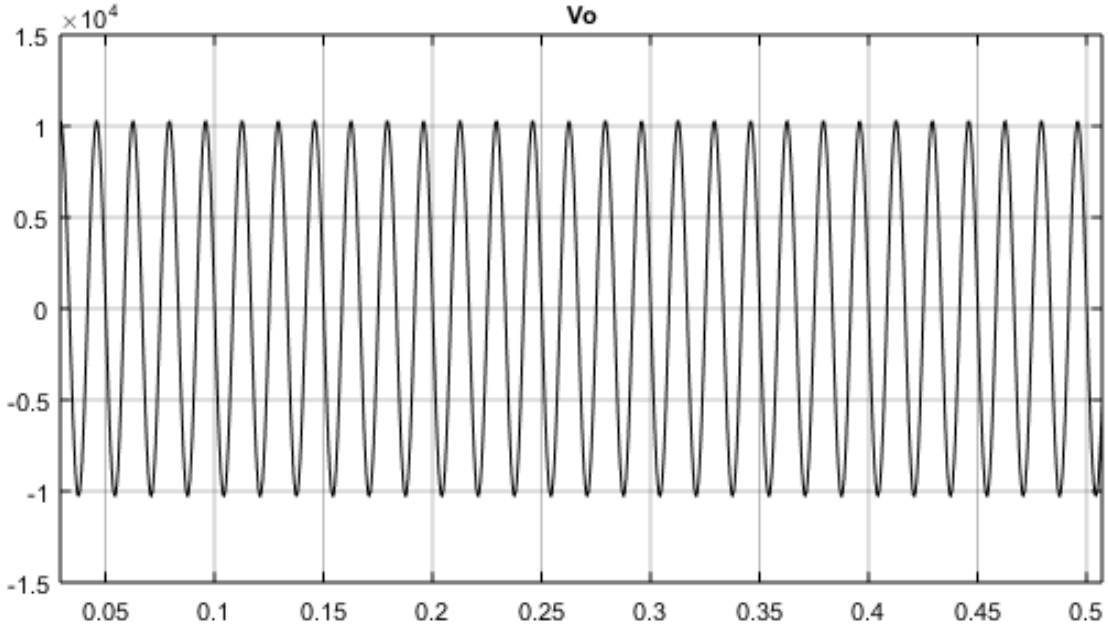


Figure 10.12: Filtered output voltage waveform for D=0.75

Simulation results verifying the operation of the converter for duty ratio of D=0.25 and D=0.75 are presented in figures 10.11 and 10.12. These simulation results prove the

working principle as well as efficacy of the Center-Point-Clamped Direct AC-AC Ćuk Converter.

CHAPTER 11 : CONCLUSIONS

Historically, PWM based direct ac-ac power converters have started to play an increasingly prominent role in Custom Power and Flexible AC Transmission Systems (FACTS) applications. In comparison with indirect ac-ac power converters, direct ac-ac power converters are smaller due to lack of bulky capacitors that are used in indirect ones to store energy in the intermediate stages. Also, they are cheaper due to the lack of intermediate stages which are present in indirect ones. These intermediate stages require more power semiconductor devices as well as reactive components. But the implementation of the prevalent direct ac-ac converters by utilities remains challenging due to lack of availability of power semiconductor devices at utility scale voltage and power ratings.

The novel topology of Center-Point-Clamped AC-AC Direct Power Converter offers a unique technique to employ power semiconductor devices rated at lower voltage and power ratings for direct ac-ac power converters rated at utility scale voltage and power ratings. This thesis analyzes afore mentioned novel topology of converter that offers a clamp to mid-voltage point at the source. It may be seen that proposed topology reduces voltage stress on power devices by half and improves the harmonic spectrum at the output. Simulation as well as experimental results verifying the operation of proposed configuration has been presented in this thesis. Overall system design including the power circuit design, dynamic analysis, and controller design has also been discussed

here. An input filter has also been designed for the prevention of switching harmonics from being introduced into the input power source.

Dynamic analysis is performed using state space averaging and small signal perturbation techniques and system transfer function is derived. A compensator is designed to improve the dynamic characteristics of this converter and simulations are performed to evaluate the efficacy of this controller. It is shown that the converter reaches steady state within two-three fundamental cycles when reference voltage is changed instantaneously. Simulation results along with experimental waveforms illustrating operating point change, line and load regulation are also presented in the paper which further indicates the robustness of the designed closed loop controller.

Finally, a novel family of center-point-clamped ac-ac direct power converters has been introduced in this thesis. This family of power converters can be used to construct power quality devices at utility scale voltage and power ratings with low voltage and power rated semiconductor devices, thereby increasing the cost efficiency as well as power transfer efficiency of power quality devices.

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