ENHANCED ELECTRON MOBILITY AT Gd_2O_3(100)/Si(100) INTERFACE: ORIGIN AND APPLICATIONS

by

Wattaka Sitaputra

A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Optical Science and Engineering

Charlotte

2012

Approved by:

_____
Dr. Raphael Tsu

_____
Dr. Michael A. Fiddy

_____
Dr.Yong Zhang

_____
Dr. Na Lu

ABSTRACT

WATTAKA SITAPUTRA. Enhanced electron mobility at Gd_2O_3(100)/Si(100) interface: origin and applications. (Under the direction of DR. RAPHAEL TSU)

A growth of a gadolinium oxide (Gd_2O_3) layer with (100) orientation on a Si(100) substrate was obtained for the first time using molecular beam epitaxy deposition (MBE) with the growth temperature in the range of 150-200°C and the oxygen partial pressure in the range of 10^{-7}-10^{-6} Torr. The growth was performed on three type of Si(100) substrate; n-type, p-type, and intrinsic. Among the three major orientations, i.e. (111), (110) and (100), the Gd_2O_3(100) is known from energetic point of view to be least favorable. Nonetheless, an enhancement in electron mobility can only be found from the interface between Gd_2O_3(100) and Si(100). Although p-type Si(100) results in the best structural considerations from x-ray diffraction among the three types of substrate, the best feature was observed in the Gd_2O_3(100)/n-type Si(100) because of its highest mobility enhancement and satisfactory structural stability. The mobility of 1670-1780 $cm^2/V{\cdot}s$ was observed at room temperature, for carrier concentration > $10^{18}cm^{-3}$. This amounts to a factor of four higher in electron mobility compared to a heavily doped n-type substrate with similar carrier concentration. This accumulation of electrons and mobility enhancement are attributed to two-dimensional confinement from charges transfer across the interface quite similar to modulation doping. Owing to these properties, the Gd_2O_3(100) becomes a promising candidate in promoting the scaling of logic devices.

ACKNOWLEDGEMENT

I would like to show my gratitude to a number of individuals who have been my support for the past three years. Without guidance and encouragement from Dr.Raphael Tsu, I would not have made it this far in my doctoral degree. It was my greatest fortune that I had a chance to learn from him how to understand physics in such a simple way. His unique ways of understanding physics passing down to me have inspired fascinating ideas throughout my Ph.D career. Our exchange of ideas has been one of the enjoyable moments.

I am also greatly indebted to Dr. Michael A. Fiddy and Dr. Na Lu who take an important part in helping me to start my Ph.D journey. Special thanks go to Dr.Yong Zhang who was willing to participate in my final defense committee.

I would like to give special thanks to Mr. John Hudak who has been helping me with all the necessities that I need for my experiment throughout the years. I am also grateful to several professors through the classes.

Among my friends, Warinya Chemnasiri and Nian Chen have provided me with joy and support for enrichment of my life during my time at the University of North Carolina at Charlotte (UNCC).

I am grateful with deepest gratitude to my family in Thailand as well as those in United States, Lanier and Karen Ellis, for giving me their unyielding love and support.

Finally, I would like to acknowledge the financial, academic and technical support from the University of North Carolina at Charlotte and its staffs, especially the financial aid, GASP program, that makes it possible for me to engage in the Ph.D program at UNCC.

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION

1.1 A Need in High-K Dielectric for Future Devices

To comply with the on-growing demand in miniaturizing the electronic devices, technologies involved in scaling down in size post challenging requirement on both tools and materials. As the feature size is reduced, some of the physical properties of the material require special considerations. These effects appear most prominently in the scaling down of a metal-oxide-semiconductor field-effect transistor (MOSFET), including amplifiers with high input impedance as well as analog switches and digital integrated circuits.

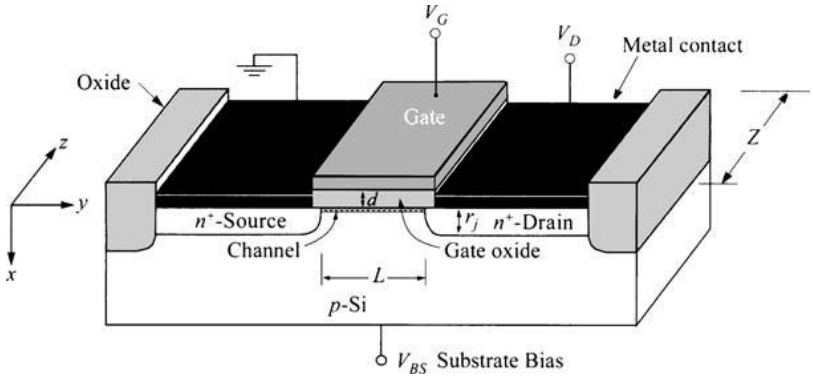

Figure 1. Schematic diagram of a planar MOSFETs structure [1]

A simple geometry of a planar MOSFET can be seen in figure 1. It comprises heavily doped regions (source and drain), a thin oxide layer (gate dielectric), and metal contacts. Specifically, the metal contact at the gate dielectric is called gate. In the integrated circuit, each MOSFET is isolated from one another by a thick layer of oxide

called field-oxide. Important parameters that will be used to discuss characteristics of the MOSFET are; the channel length (L), channel width (Z) and oxide thickness (d).

There are many ways to classify the type of MOSFET. For instance, MOSFETs can be categorized into enhancement and depletion mode, based on the state of the transistors when the gate bias is zero. In the enhancement mode MOSFET, the transistors stay in an off-state when there is no gate voltage applied. On the other hand, the depletion mode transistors stay in an on-state even if the gate voltage is zero. The relationships between the drive current (I_D), drain bias (V_D) and gate bias (V_G) of different types of MOSFET are illustrated in figure 2. It will be illustrated later on that the use of a $Gd_2O_3(100)$ as a gate dielectric can be beneficial to both enhancement and depletion mode MOSFETs.

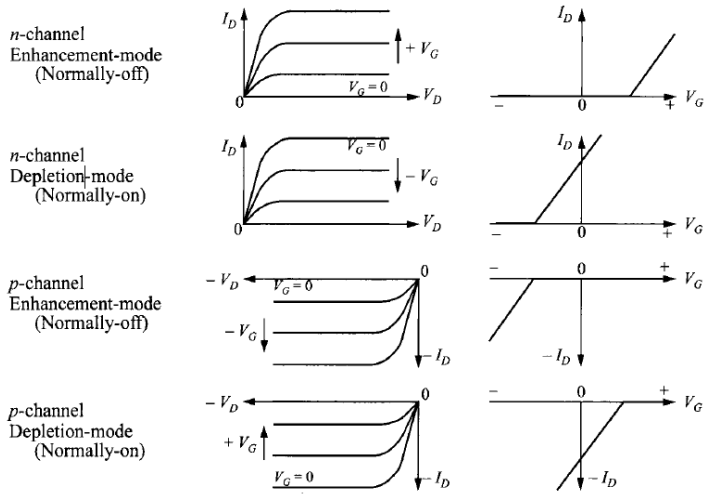

Figure 2. Relationship between the drive current (I_D), drain bias (V_D) and gate bias (V_G) of n- and p-channel MOSFETs in enhancement and depletion mode [1]

For simplicity, characteristics of the enhancement mode will be used to illustrate major differences between a long channel and short channel MOSFET. At a constant gate

voltage above the threshold voltage (V_T), the characteristic of the drain current can be divided into three region, linear, non-linear and saturation region. In the linear region of the long channel MOSFET, the drain current is a function of the voltage drop across the source-drain junction (V_D) and can be written as;

$$I_D = \frac{\mu_s Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}{V_D}^2\right] \quad (1)$$

where μ_s is a surface carrier mobility (which is not the same as the bulk), and C_i is the dielectric capacitance. As shown in figure 2, the drain current does not increase infinitely but saturate when the condition (V_G-V_D) < V_T is met. A pinch-off occur near the drain terminal due to a reduced relative voltage between gate and semiconductor. Therefore, the inversion layer is cut-off as can be seen in figure 3. In such case, the drain current no longer depends on the V_D and can be written as;

$$I_{D,sat} = \frac{\bar{\mu}_n Z C_i}{2ML}(V_G - V_T)^2 \quad (2)$$

where M is a function of substrate doping concentration and the oxide thickness [1]. It can be seen from Eq.1 and 2 that a higher drive current can be obtained through the increase in μ_s, channel length and dielectric capacitance.

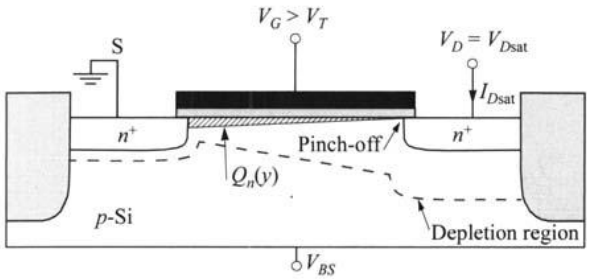

Figure 3. Schematic diagram illustrating pinch-off of the inversion layer at $V_D = V_{Dsat} = V_G - V_T$. [1]

The constant mobility approximation works well in the long channel limit and the characteristic of the drain current follows the previous equations. However, as the device becomes smaller, the separation between source and drain terminal become close enough that the depletion region from the two overlap. This causes the drain-induced barrier lowering which increase the leakage current in an off-state[1, 2]. In addition, this shortened source/drain separation also increases the longitudinal electric field (source-drain bias) to be comparable to the vertical electric field (gate bias). In such case, the constant mobility approximation is no longer accurate since the carrier mobility becomes a function of drain bias. This causes the drain current to saturate at a lower drain bias due to the reduction in carrier mobility at high longitudinal field. As a result, a maximum drive current as well as the on/off ratio is lowered. Furthermore, the carriers, especially electrons that travel near the drain terminal, also gain a kinetic energy from a high longitudinal electric field. These highly energetic electrons, called hot electron, can cause a shift in threshold voltage and degrade the device over time. In order to alleviate the problems from short-channel effect and preserve characteristics of long channel MOSFETs, a higher substrate doping is required to reduce the depletion width of the source and drain. However, as the channel doping concentration increases, the threshold voltage is also increased. Thus, a thinner oxide is required to maintain a reasonable threshold voltage. As the change in one parameter affects others, a scaling rule such as the one presented in table 1 must be used.

It is desirable to keep the field constant along the path of scaling. However, not every parameter can be scaled accordingly. As a result, the increase in electric field becomes unavoidable. Although techniques such as retrograde channel doping profile and

two-step source/drain junction [3-6], have been proposed to solve the short channel effect, the undesirable behaviors still occur due to limitation on scaling of each parameter as follow: (1) the reduction in junction depth results in increasing series resistance, (2) the lower threshold voltage comes with a higher off current, (3) too high substrate doping will cause a junction breakdown as well as a decrease in carrier mobility, (4) a demand for higher speed as well as system consideration slows down the scaling in supply voltage, (5) the reduction in oxide thickness is limited by an increase in direct tunneling. Nonetheless, there are two promising technologies that could advance the scaling, which are three-dimensional structure on ultra-thin body silicon-on-insulator (SOI) and high-κ gate dielectric with metal gate.

Table 1. Scaling factor and limitation for different parameters in ideal constant-field and reality[1]

Parameter	Scaling factor: Constant field	Scaling factor: Actual	Limitation
L	1/K	-	-
Field	1	> 1	-
d	1/K	> 1/K	Tunneling, Defects
Junction depth	1/K	> 1/K	Resistance
V_T	1/K	>> 1/K	Off current
V_D	1/K	>> 1/K	System, V_T
Substrate doping	K	< K	Junction breakdown

Figure 4 shows a scaling trend for high performance, low operating power, low standby power and III-V/Ge logic devices according to International Technology Roadmap for Semiconductor (ITRS) 2011. It can be seen that the demand in an even smaller device is reflected directly onto the gate length which is expected to be as short as 10 nm in nine years. On the other hand, the drive current is expected to increase with a

lower supply voltage while maintaining the same off current. The devices with III-V/Ge as a channel have been a goal for the industry owing to their much higher carrier mobility than silicon. However, much work still needs to be done due to fabrication and processing difficulty.

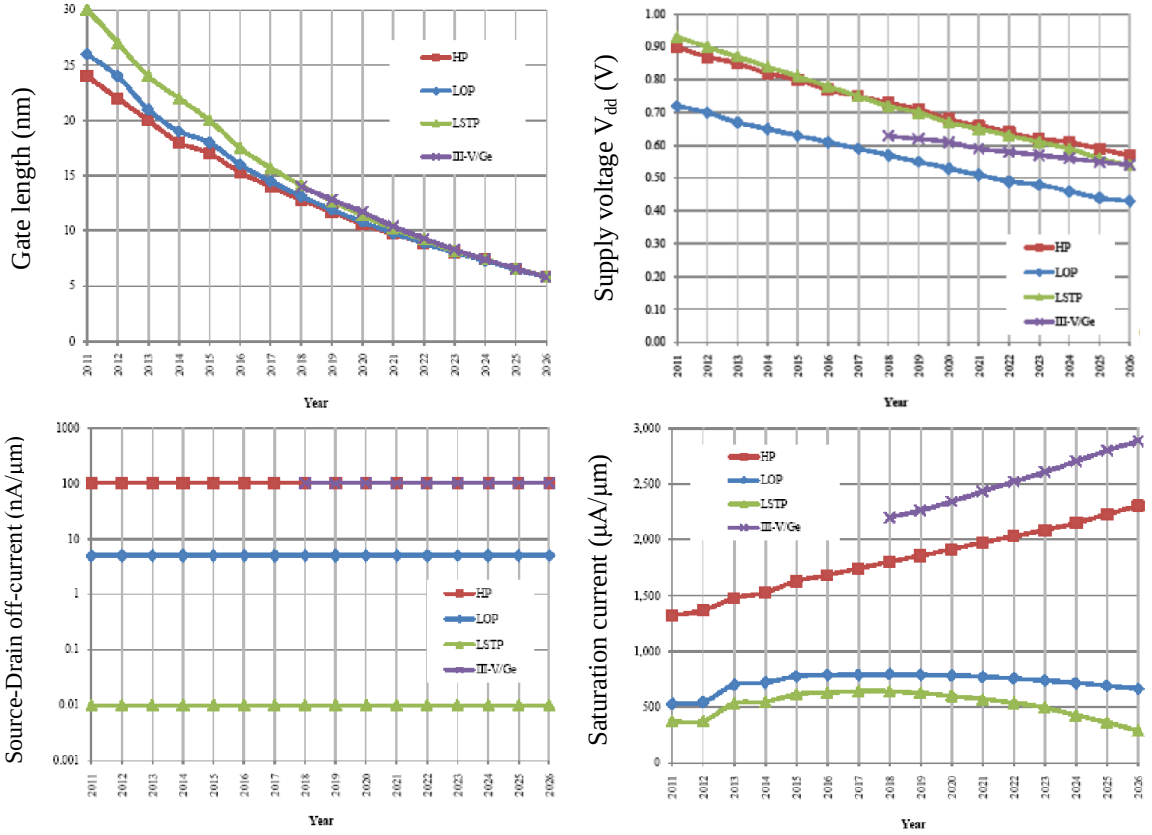

Figure 4. ITRS 2011 scaling trend of logic technologies with year; (a.) Gate length, (b.) Supply voltage, (c.) Off-current, (d.) Saturation on-current. (HP = High Performance, LOP = Low Operating Power, LSTP = Low Standby Power) [7]

To follow the scaling trends, the research on high-κ dielectric, i.e. Gd_2O_3, has been engaged. As mentioned previously, the oxide thickness must be decreased in order to compensate the increase in threshold voltage due to the higher channel doping in short channel devices. By reducing the gate oxide thickness, the oxide capacitance as well as

the charge density within the inversion layer increases at the same gate bias. In other words, the same amount of charge within the inversion layer can be induced with a lower gate bias. This capacitance of the gate oxide can be calculated from;

$$C_i = \frac{\epsilon_o \kappa A}{d} = \frac{dQ}{dV} \tag{3}$$

where ϵ_o is a free space permittivity (8.85 x 10^{-12} F/m), κ, a dielectric constant, and A is the gate area. The high-κ gate dielectric not only alleviates the problem with threshold voltage but also solve the problem with direct tunneling. A thickness limit before the direct tunneling becomes significant for a SiO_2 gate oxide is approximately 2 nm[1]. To prevent this, the SiO_2 must be replaced by another high-κ insulating material with sufficiently large band gap and a high enough conduction band and valence band offset (approximately 2 eV). It can be seen from Eq. 3 that the same capacitance can be obtained with a thicker layer if a material with higher κ were used. A terminology, equivalent oxide thickness (EOT), was created in order to associate a physical thickness of the high-κ dielectric with an equivalent SiO_2 thickness that gives the same capacitance. It can be written as;

$$EOT = d_{high-\kappa}\left(\frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}}\right) \tag{4}$$

A sufficiently high dielectric constant allows the use of a thicker gate oxide to prevent the direct tunneling while maintaining the same or even higher capacitance as well as the drive current. Many oxides, such as Al_2O_3, HfO_2, ZrO_2, Y_2O_3, Ta_2O_5, TiO_2 as well as lanthanide oxides, have been investigated as a candidate in replacing the SiO_2 [8-14]. However, only few were proved to be useful due to a stringent requirement in processing and compatibility with silicon. It should also be noted that the larger dielectric

constant typically results in a smaller band gap, and vice versa, as can be seen in figure 5-a. Thus, materials with extremely high dielectric constant are not always favorable. There are six factors that must be considered in choosing the high-κ dielectric[9].

1. It must have a sufficiently high dielectric constant in order to provide a sub-nanometer EOT. According to ITRS 2011, the high dielectric constant (κ) of the new material should be greater than 30 for high-performance future devices.
2. It must be thermodynamically stable on silicon.
3. It must be able to withstand high temperature processing that is required along the fabrication process without forming an interfacial layer or changing its phase.
4. It must have a proper conduction and valence band offset to minimize the gate leakage current.
5. Trap states at the interface must be sufficiently low.
6. It must not contain high electrically active bulk defects.

Figure 5-b shows conduction and valence band offset of various oxides with respect to the silicon band gap. It is crucial to have both offset greater than 1 eV to lower the gate leakage current. Some high-κ oxides such as TiO_2 and $SrTiO_3$ have a very large dielectric constant, > 60 for TiO_2 and >300 for $SrTiO_3$ [8, 9], but the conduction band offset with respect to the silicon is almost zero. Thus, they are not suited to be used as a gate dielectric. Among all the candidates, only hafnium oxide (HfO_2) made it into a production line [15]. In 2007, the SiO_2 was replaced with the HfO_2 for the first time in 45 nm microprocessor technology. Later on in 2010, 32 nm core processors (Core-i3, i5 and

i7) were released by Intel using the same HfO_2. Nonetheless, the HfO_2 still has drawback which occur during the source/drain formation which requires high temperature processing. Due to its low crystallization temperature, the HfO_2 layer crystallizes during the fabrication process and change the structure from amorphous into a poly-crystalline with predominantly monoclinic structure. This leads to an increase in leakage current through the grain boundary [16]. Incorporation of other elements into the HfO_2 structure was proposed as a mean to increase the crystallization temperature and reduce the leakage current [17-20]. Nonetheless, the amorphous dielectric is still not a satisfactory solution in a long term due to manufacturing difficulty in growing a thin-film with sufficiently low defect density [21-23].

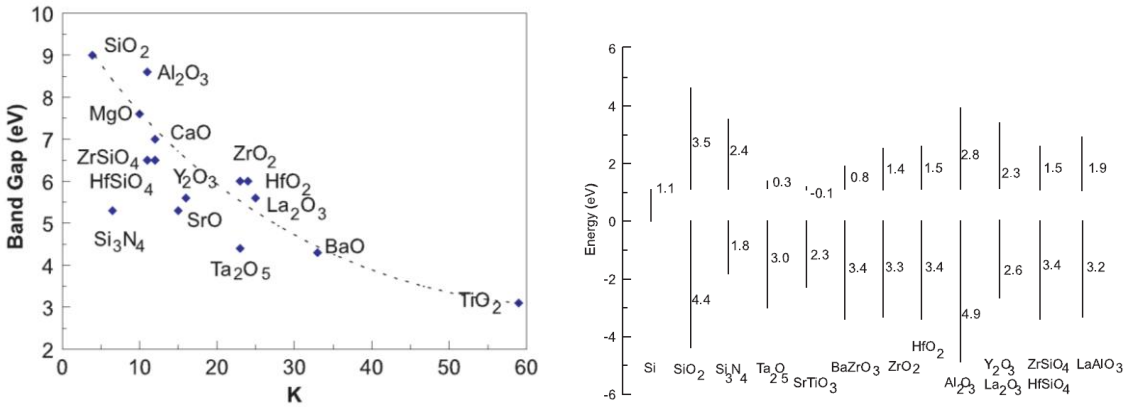

Figure 5. Diagrams illustrating (a) a relationship between band gap and dielectric constant of candidate oxides, and (b) conduction and valence band offset with respect to silicon.[9]

Another solution could be achieved by replacing the amorphous oxide layer with a crystalline layer. This way, the crystallization temperature will no longer be a problem. However, the choice of material is further limited depending on the substrate lattice parameter and chemistry. In order to grown the epitaxial layer, the lattice matching

between the oxide layer and the substrate should be better than 3% [24]. The lattice mismatch is defined as;

$$\Delta a = \frac{a_{oxide} - a_{Si}}{a_{Si}} \tag{5}$$

where a_{oxide} is a lattice constant of the oxides and a_{Si} is a lattice constant of the silicon. A summary of lattice mismatch between silicon and candidate oxides is illustrated in table 2.

Table 2. Summarize of the band gap and lattice parameters of the candidate oxides as well as its lattice matching with respect to silicon [8, 9, 14, 24, 25]

Crystal Structure	**Composition**	**Lattice parameter (Å)**	**Matching parameter**	**Lattice mismatch (%)**	**Band gap (eV)**
Diamond	Si	5.431	/	/	1.1
Rock-salt	BaO	5.534	$a_{Si} : a_{ox}$	+1.8	4.4
	SrO	5.14	$a_{Si} : a_{ox}$	-5.3	5.3
Fluorite	CeO_2	5.411	$a_{Si} : a_{ox}$	-0.36	3.3
	ZrO_2	5.148	$a_{Si} : a_{ox}$	-5.2	5.8
Perovskite	$SrTiO_3$	3.905	$a_{Si} : a_{ox}\sqrt{2}$	+1.7	3.3
	$BaTiO_3$	4.01	$a_{Si} : a_{ox}\sqrt{2}$	+4	2
	$LaAlO_3$	3.81	$a_{Si} : a_{ox}\sqrt{2}$	-0.7	6.2
	$SrHfO_3$	4.069	$a_{Si} : a_{ox}\sqrt{2}$	+5.9	6.5
	$LaScO_3$	4.128	$a_{Si} : a_{ox}\sqrt{2}$	+7.5	5.9
Bixbyite	Pr_2O_3	11.152	$a_{Si} : a_{ox}/2$	+2.7	3.9
	Y_2O_3	10.604	$a_{Si} : a_{ox}/2$	-2.4	6
	Gd_2O_3	10.813	$a_{Si} : a_{ox}/2$	-0.45	5.8
	Nd_2O_3	11.08	$a_{Si} : a_{ox}/2$	+2	5.8
	La_2O_3	11.32	$a_{Si} : a_{ox}/2$	+4.2	5.5
Spinel	γ-Al_2O_3	7.91	$a_{Si} : 2a_{ox}/3$	-2.9	8.8

Many rare-earth oxides exhibit a decent lattice matching, and proper band gap and bandedge offset with respect to silicon. However, rare-earth metals listed in table 2, except Gd, La and Nd, can exhibit more than one oxidization states leading to phase

segregation during the growth. This fact also applies to some oxide with fluorite structure such as CeO_2. With all the constraint being considered, only BaO, $LaAlO_3$, and Gd_2O_3 pass the selection. Among the three, the Gadolinium oxide (Gd_2O_3) emerges as the best candidate for replacing the SiO_2 because of its superior lattice matches to the silicon compare to both $LaAlO_3$ and BaO. The $LaAlO_3$ also has a flaw in its high growth temperature, > 700°C [26]. At such high temperature, maintaining an abrupt interface is difficult in term of promoting inter-diffusion at the interface between the substrate and the deposited film. In addition, the Gd_2O_3 has a reasonably large band gap of 5.98 eV and a proper conduction and valence band-offset with respect to silicon of 2.08 eV and 2.78 eV, respectively [25]. A dielectric constant of the Gd_2O_3, 13-24 [8, 9, 13, 17, 24], is also within an acceptable range. Together with a thermodynamic stability with the silicon, the Gd_2O_3 complies with the requirements imposed by further scaling. Extensive studies has been made and a high quality epitaxial growth of Gd_2O_3(111) on Si(111) has been reported together with the method of growing a double-barrier quantum structure by Osten and Fissel group [27, 28]. However, the industry is built on Si(100). The epitaxial growth of (110)-oriented Gd_2O_3 on Si(100) was reported by the same group [11, 29]. This epitaxial growth of Gd_2O_3(110) on Si(100) is more favorable during the deposition at high temperature (600-700˚C), due to its lower surface energy and alternative lattice matching, compare to the growth of Gd_2O_3(100). Nevertheless, the growth of the Gd_2O_3(100) on Si (100) has its own merit in term of substantial increase in electron mobility. Mainly for this reason, we have embarked on the growth of Gd_2O_3(100). In addition, the Gd_2O_3 with (100) orientation is considered to have a polar surface with a non-zero net dipole moment perpendicular to the surface. This structure with non-zero

macroscopic dipole moment is ferroelectric material. It could be a candidate material for ferroelectric FETs [30-32]. However, this orientation contains the highest surface energy among the three major orientations due to the contribution of electrostatic energy from the dipole which increases as a function of the thickness [33-35]. As a result, a thick layer of Gd_2O_3(100) is generally unstable unless the charge compensation mechanism is introduced as a mean to lower the energy of the system. Through this mechanism, a charge reconfiguration across the interface induces an enhancement in carrier mobility quite similar to the well-known $LaAlO_3/SrTiO_3$ heterostructure [36, 37].

Typically, the carrier mobility of the MOSFETs with the high-κ dielectric is inferior to the MOSFETs with SiO_2 due to the higher interface trap density and a strong remote phonon and Coulombic scattering [38]. Thus, the epitaxial growth of the (100)-oriented Gd_2O_3 on Si(100) which provides the enhancement in electron mobility becomes a better candidate than the Gd_2O_3(110) in realizing a better performance in term of the speed, drive current and power density.

What follows is presented with confirmation of our model with all the necessary structural and electrical characterization by x-ray diffraction and hall measurement.

CHAPTER 2: CONCEPTUAL MODEL OF Gd_2O_3(100)

2.1 Possible Growth Mode of Gd_2O_3 on Silicon Using Mbe

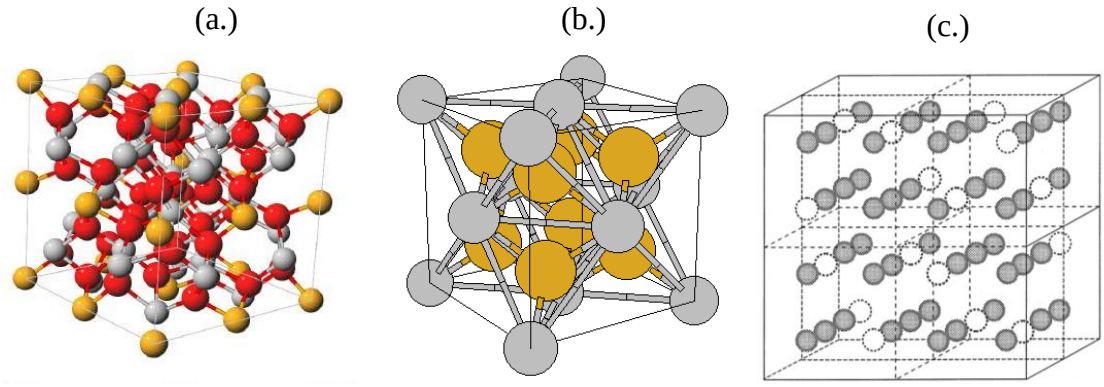

Figure 6. Illustration of (a.) cubic bixbyite structure [Gray = Gd^{3+}, Red = O^{2-}, Yellow = surface Gd^{3+}], (b.) fluorite structure [Gray = cation (Ce^{2+} or Ca^{2+}), Yellow = anion (O^{2-} or F^{2-})], and (c.) positions of oxygen (gray sphere) and oxygen vacancies (hollow sphere) within the cubic bixbyite unit cell [39-41]

Gadolinium oxide (Gd_2O_3) is a member in lanthanide oxide family, oxides of metallic element with atomic number 57-71. The lanthanide oxides could occur in different structural phase such as cubic bixbyite, hexagonal or monoclinic. Because of this property and several oxidization state of rare-earth metal, many lanthanide oxides fail to become a candidate for replacing the SiO_2 as they undergo structural phase transformation at high temperature which is within the range of complementary metal-oxide semiconductor (CMOS) processing [11]. The Gd_2O_3, on the other hand, crystallizes in stable cubic bixbyite structure, space group $Ia\bar{3}$, when it is deposited onto a single crystal silicon substrate (figure 6-a). This structure is a combination of eight fluorite unit

cells (figure 6-b) with two oxygen vacancies within each fluorite cell. The positions of the oxygen and oxygen vacancies in the cubic bixbyite structure are illustrated in figure 6-c.

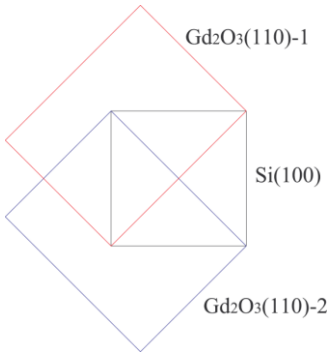

Figure 7. Illustration of alternative lattice matching between two domain of Gd_2O_3(110) and Si(100)

Although the atomic arrangement of the cubic bixbyite structure is different than diamond structure of silicon, an epitaxial growth of the Gd_2O_3 on Si can still be obtained in some directions because of their lattice matching within 0.5% and in-plane rotation. An epitaxial growth of (111)-oriented Gd_2O_3 on the Si(111) substrate with A/B twinning relationship, where B orientation of the Gd_2O_3(111) is 180° rotated around a surface normal with respect to A orientation of silicon, can obtained when the substrate temperature is higher than 600°C [11]. In contrast, a significant faceting due to the formation of a structure with lower surface energy, such as Gd_2O_3(111), was found in the growth of the Gd_2O_3 on Si(110) instead of an epitaxial growth of the Gd_2O_3(110) [42]. As for the growth on Si(100) substrate, the epitaxial growth of Gd_2O_3(110) is the most favorable growth mode [43]. This type of epitaxial growth also applies to other lanthanide oxides with fluorite or cubic bixbyite structure [35, 43, 44]. There are three

supporting factors behind this particular epitaxial growth. First, the growth with (100) orientation has the highest surface energy among the three orientations. Second, a strong Si-O bonds and a highly ionic Gd-O bond makes the Si-O-Gd bonding more likely to occur than the Si-Gd-O bonding [45]. Third, the oxygen atoms that are bonded to the silicon surface atoms rearrange itself along the direction of a (2x1) reconstructed dangling bond of the silicon [12]. The inter-atomic distance between these oxygen atoms within the first plane is lattice matched with the Gd_2O_3(110) with 45° in-plane rotation relative to the substrate as shown in figure 7.

This epitaxial growth of the Gd_2O_3(110), however, consists of two orthogonal in-plane domain which share equal growth probability. With the two domains coexisting, a leakage current or atomic diffusion, which could degrade electronic devices, would be promoted along their grain boundary. Though, it was found that a single domain Gd_2O_3(110) can be grown on the Si(100) with 4° miscut [46]. This epitaxial growth of the Gd_2O_3(110) on Si(100) can only be obtained at a relatively high temperature (600-670°C). With a lower growth temperature, the Gd_2O_3(111) crystallite tends to dominate the structure as it is the structure with the lowest surface energy [47-49].

Considering the surface energy and alternative lattice matching, the growth of the Gd_2O_3(100) on Si(100) might seem unlikely but it is still possible. Since a single (100) face of the Gd_2O_3 unit cell can accommodate four of the (100) face of the Si unit cell with a fitting better than 1%, the matching of this symmetry can force the Gd_2O_3 structure to assume the (100) orientation in spite of the high surface energy. To achieve this growth, the periodic and symmetry of the silicon surface must not be altered through the surface reconstruction. In addition, a time that the incoming particles are able to diffuse along the

surface of the substrate must be long enough that they can arrange themselves according to the template or symmetry of the substrate but not too long such that they could assume the lowest energy configuration. This condition can be ensured by controlling the surface diffusion through the growth temperature. High growth temperature enhances the surface diffusion while low growth temperature reduces it. Though, a caution should be made as the deposition rate increases with the lower substrate temperature. A proper growth temperature for the Gd_2O_3(100) on Si(100) is in the range of 150-200°C. The lower temperature results in an amorphous structure while the higher temperature results in either Gd_2O_3(111) or Gd_2O_3(110) depending on temperature range.

Oxygen partial pressure is another important parameter during the growth. When the oxygen arrange themselves differently within the first layer due to partially reconstructed surface, the growth of the Gd_2O_3(100) is disrupted and populated with defects. Thus, the structure of the layer turns into either amorphous or polycrystalline with predominant Gd_2O_3(111). This problem can be alleviated by increasing the oxygen partial pressure. It should be noted that, due to the intrinsic ordered oxygen vacancies within the cubic bixbyite structure, the oxygen diffusion within this oxide becomes relatively fast. Thus, an excess oxygen supply could elevate the formation of an oxygen-rich interfacial layer [50]. Fortunately, as the growth is done at a relatively low temperature and the oxygen is introduced as a molecule, the oxidization of the silicon surface is not too aggressive. The increase in the oxygen partial pressure will help in forcing the template arrangement to dominate over other arrangement. This increase in the oxygen partial pressure needs to be accompanied by the lower growth rate as a mean to ensure that the layer does not turn into the amorphous structure. Therefore, a precise

control over the growth temperature and composition during the growth is required for the growth of the Gd_2O_3(100). A hydrogen-passivated surface, or (1x1) unreconstructed surface, also helps in preventing the formation of (110) orientation.

This type of growth is similar to a strained layer epitaxy. In this case, a strain is caused by the build-up electrostatic energy due to the non-zero net dipole moment perpendicular to the surface. The limitation on the thickness is also very similar to the strained layer. As thickness increases pass a critical point, defects are created in order to lower the energy of the system [51-53]. However, creating the defects is not the only option for stabilizing the Gd_2O_3(100) structure. In the case of polar oxide surface, the structure is stabilized through a surface charge reconfiguration which could happen in many forms. A compressive strain in the direction perpendicular to the surface or the inter-mixing between atoms at the interface can also reduce the energy of the system and stabilize the structure. Though, the most interesting mechanisms are a formation of ordered vacancies and a transfer of electrons between the interfaces as they could offer new properties that are not normally presented in typical dielectric materials.

The growth of Si onto the Gd_2O_3, on the other hand, results in Volmer-Weber (VW) growth mode due to a low surface energy of the Gd_2O_3 compare to Si [47]. Nevertheless, the growth of Si(111)/Gd_2O_3(111)/Si(111) heterostructure could be achieved using the encapsulated solid-phase epitaxy technique [28]. As the fabrication of a periodic structure such as resonant tunneling diode is not within the scope of this research, the epitaxial growth of the silicon onto the Gd_2O_3(100) was not fully engaged. Though, preliminary results showed the VW growth mode as expected.

2.2 Polar Surfaces

An ionic crystal surface can be categorized into polar or non-polar depending on stacking sequence and termination [34, 35, 54]. A surface is classified as polar when the layer cannot be made exclusively of dipole-free unit cells. It should be noted that the unit cell mentioned in this case is the smallest unit that exhibits a repeating electronic structure in the direction perpendicular to the surface (blue box in Fig. 8). As the discussion will be focused on the interaction between planes, the figure of merit will be represented as the interaction per unit area involving dipoles of two planes separated by the distance d, $\mu_s = n_s e d$, with number of electron per unit area, n_s. Using notation used by Tasker [54], figure 8-a, with zero net charges per unit area ($\sigma_s = 0$), is referred to as Type I where the net μ_s is zero. While in figure 8-b, because the adjacent planes have different σ_s, the arrangement is characterized by Type II, having a net $\mu_s \neq 0$ only when the terminating plane is different than illustrated. Another arrangement, Type-III stacking, also exhibits $\mu_s \neq 0$ as shown in figure 8-c due to alternating +ve and –ve charges on adjacent planes. Among the three types, only type III is considered to contain a non-zero net dipole moment perpendicular to the surface regardless of terminating planes. A classification of variety of structures with different surface termination is illustrated in appendix A. This classification also extends to the crystal structure with a low degree of ionicity or even crystal structure of a covalent compound. However, a caution must be made as one can no longer assign a formal charge to cations and anions. A fractional charge transfer must be used instead of an integer charge transfer. An example of this case is the (100) surface of perovskite such as $SrTiO_3$. The stacking sequence of the $SrTiO_3$, which is an alternating layer of SrO and TiO_2, implies non-polar

surface if formal charge of Sr^{2+}, Ti^{4+} and O^{2-} are assigned. Nevertheless, it was found experimentally that the (100) surface of $SrTiO_3$ exhibits a weak polar surface characteristic [55]. This results from the fact that the $SrTiO_3$ is not fully ionic. Thus, both SrO and TiO_2 layer are not necessary charge neutral.

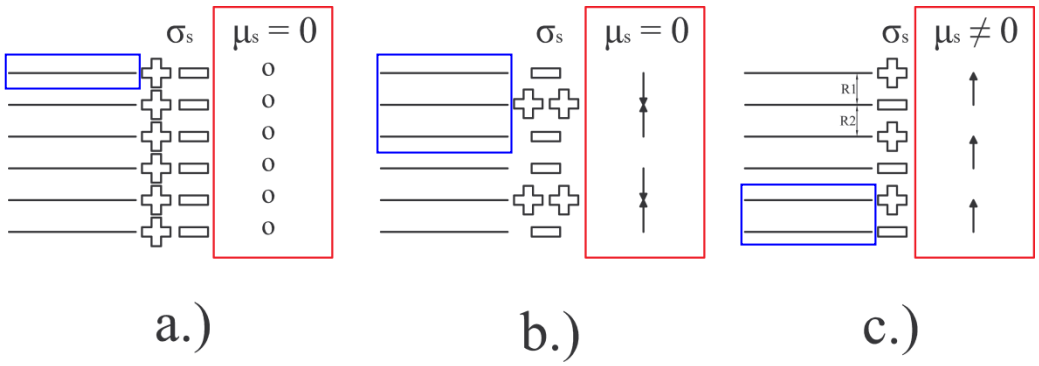

Figure 8. Three types of stacking sequence in general ionic crystal representing different charge distribution per unit area (σ_s) and net dipole moment per unit area (μ_s) perpendicular to the surface. (a) Type I with neutral planes, similar to Gd_2O_3(110) (b) Type II with charged plan but no net dipole moment perpendicular to the surface, similar to Gd_2O_3(111), and (c) Type III contains net dipole moment perpendicular to the surface, similar to Gd_2O_3(100).

In this work, the main focus is on the structure of the gadolinium oxide (Gd_2O_3) with a polar surface. In term of ionicity, the gadolinium and oxygen atom has an electronegativity of 1.20 and 3.44. With the difference in the electronegativity of 2.14, the Gd-O bond is considered to be highly ionic. Thus, the stacking sequence of the Gd_2O_3 can be classified with Tasker's notation. As there is no report on the classification of the Gd_2O_3 surface, research on the base unit of the cubic bixbyite unit cell, i.e. fluorite structure such as CaF_2 or CeO_2, was used as a guideline in assigning the surface type to different orientation of the Gd_2O_3.

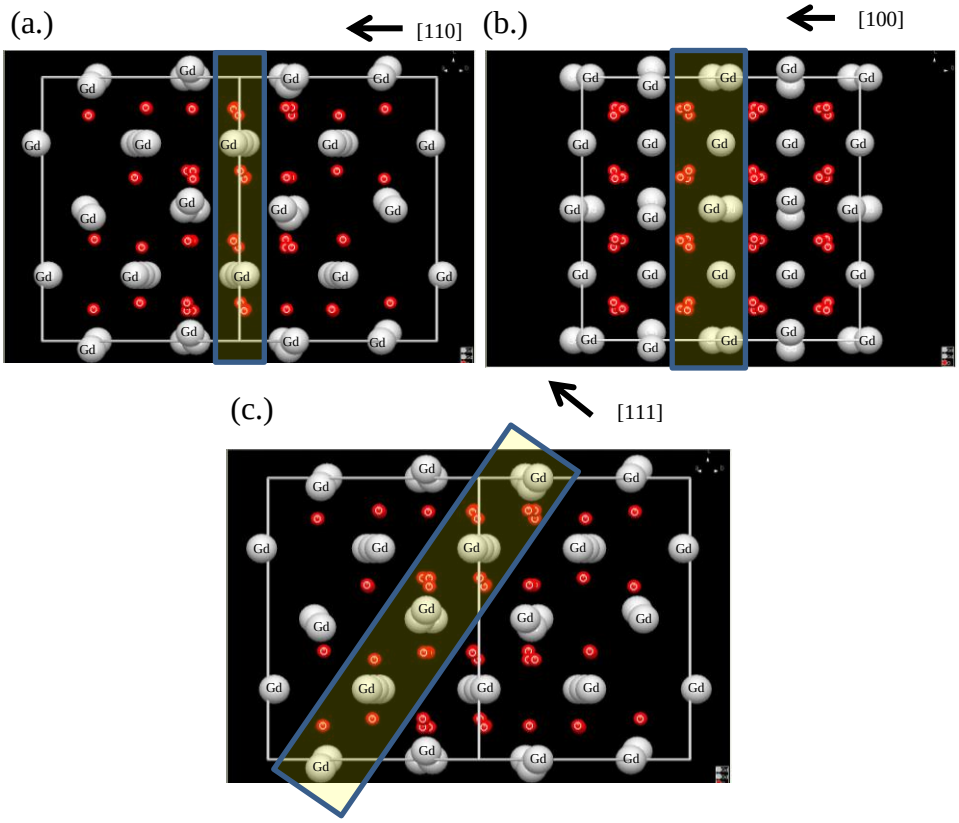

Figure 9. Illustration of the (a.) (110) plane, (b.) (100) plane and (c.) (111) plane within the Gd_2O_3 cubic bixbyite structure [56]

As can be seen in the table A1 of appendix A, the CaF_2 structure with the (110) plane as a terminating surface is classified as Type I, which is a non-polar surface. The (111) surface, on the other hand, can exhibit either polar or non-polar surface depending on termination unlike the (100) surface which exhibits the polar surface nonetheless. Due to a high surface energy from the electrostatic contribution of the polar surface, the non-polar (111) surface is more likely to grow as a predominant growth mode. This statement coincides with the report on the lowest surface energy of the CeO_2(111) [47-49]. As a result, the structure with (100) surface becomes the only growth orientation that exhibits the polar surface. The consistency of this comparison with the fluorite structure is

verified in figure 9. In this figure, the crystal structure of the Gd_2O_3 unit cell is demonstrated from different angles. The crystal planes, highlight with a yellow box, can be categorized into three stacking types which matches with the previous statement. The (100)-oriented Gd_2O_3 has alternating layers of Gd^{3+} and O^{2-} which is classified as Type III, while the other orientations such as the Gd_2O_3(110) and Gd_2O_3(111) are classified as type I and II, respectively.

2.3 Instability of Polar Surfaces

One major concern for the polar surface is its instability. In an ideal semi-infinite crystal structure with the polar surface, the structure is not stable due to a high surface energy. The majority of the surface energy in this case can be attributed to the electrostatic energy contributed by the non-zero dipole moment perpendicular to the surface. This effect can be illustrated using the crystal with type III ionic stacking. Assuming that the each plane of type III ionic crystal contains a uniform charge per unit area of $\pm\sigma_s$ as illustrated in figure 8-c, the dipole moment per unit area from each bi-layer (μ_s) is proportional to;

$$\mu_s = \sigma_s R_1 \tag{8}$$

and the net dipole moment for N unit cell becomes

$$\mu_N = N\sigma_s R_1 \tag{9}$$

By treating the bi-layer of the unit cell as a parallel plate capacitor, the increase in electrostatic potential (in cgs unit) contributed by each repeating unit can be written as

$$\delta V = 4\pi\sigma_s R_1 \tag{10}$$

which is in the range of tens of eV for a highly ionic materials [34]. The increase in electrostatic potential as a function of thickness can be seen in figure 10-a. The electrostatic energy per unit area contributed by these dipoles becomes

$$E = 2\pi N R_1 {\sigma_s}^2 \tag{11}$$

From Eq. 9 and 11, in a semi-infinite crystal where $N \to \infty$, both net dipole moment perpendicular to the surface and electrostatic energy approach infinity. As this occurs, the system becomes unstable. Therefore, a cancelation of the macroscopic dipole moment is required in order to reduce the energy of the system.

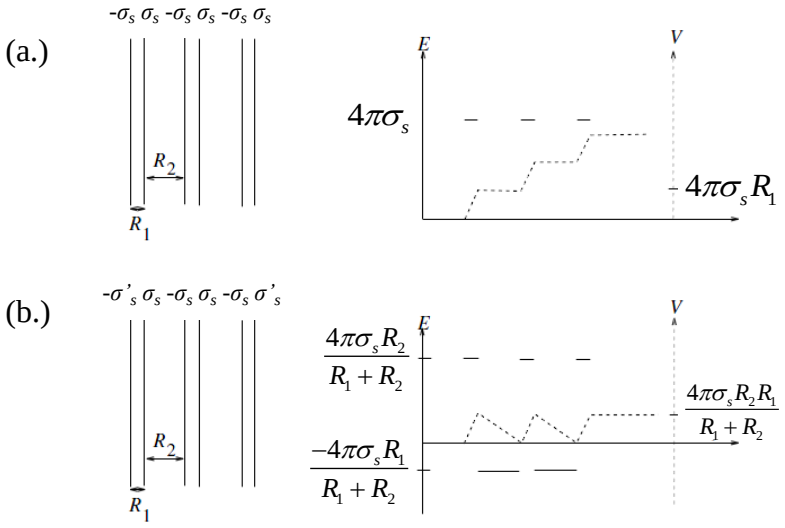

Figure 10. Diagrams illustrating relationships between electric field, electrostatic potential and a thickness in the direction perpendicular to the surface of the (a.) uncompensated and (b.) compensated polar surface. [34]

In figure 10-b, the divergence of potential and energy is suppressed by modifying the terminating plane such that it contains the charge density of $\sigma_s' = \frac{\sigma_s R_2}{R_1+R_2}$. With this termination, the charge density of $-\frac{\sigma_s R_2}{R_1+R_2}$ of the left-most plane will couple with the same amount of positive charge density on the adjacent plan to the right. Then, the remaining charge density of $\frac{\sigma_s R_1}{R_1+R_2}$ on the second plane will couple with the charge density of $-\frac{\sigma_s R_1}{R_1+R_2}$ of the thrid plane and so on. As a result, the dipole moment no longer points in the same direction, or increases monotonically. After the summation of all the dipole moment from six layers, the total dipole moment per unit area in this example becomes $\frac{\sigma_s R_1 R_2}{R_1+R_2}$. It can be seen that the macroscopic dipole moment no longer depends on thickness. As a result, the divergence of the electrostatic potential and the surface energy

are eliminated. A general form of the surface charge reconfiguration when more than one layer is modified can be written as;

$$\sum_{j=1}^{m} \sigma_j = -\frac{\sigma_{m+1}}{2}\left[(-1)^m - \frac{R_2 - R_1}{R_2 + R_1}\right] \tag{12}$$

where m is the number of modified layer, j is the order of modified layer (with 1 as the outermost layer), $\sigma_j \neq \sigma_s$ for $1 \leq j \leq m$, and $\sigma_{m+1} = \sigma_s$.

From this equation, if the structure of interested exhibits a polar surface with equally spaced atomic planes ($R_1 = R_2$), the summation of the charge density over the modified layers must be equal to half of the bulk charge density on each plane. This condition opens up several possibilities for the charge compensation mechanism that can occur to cancel out the polarity.

2.4 Charge Compensation Mechanisms

Mechanisms that can suppress the divergence of electrostatic potential and surface energy as well as nullify polarity of the polar surface are called charge compensation mechanism. This mechanism includes any physical process that can provide a depolarizing field and stabilize the system, e.g. adsorption of foreign atoms or ions, partial filling or emptying of surface electronic states, and modification of surface stoichiometry (reconstruction). Through these mechanisms, wide ranges of phenomena are originated. It should be noted that the charge compensation mechanism occurs not only on the surface but also any point of polar discontinuity. An interface is another location that the polar discontinuity can be found. When the crystal structure with the polar surface comes into contact with a non-polar structure or a polar structure with different macroscopic polarization, a polar interface is formed between them. The charge compensation mechanism at this polar interface can be different than the surface depending on the involved charged particles. For instance, a partial filling of the electronic states can occur at the interface while the adsorption of the foreign atoms and structural reconstruction take place at the surface. In addition, the number of mechanisms that occur is not limited to just one at a time.

Because of these charge compensation mechanisms, some useful properties for MOSFET applications such as high carrier concentration and mobility can be observed at the interface of some well-known heterostructures, i.e. $LaAlO_3/SrTiO_3$ (LAO/STO) and AlGaN/GaN [36, 57-62]. A modulation of charge density at the interface by external electric field as well as the ferromagnetic order was also reported for the LAO/STO

system[63, 64]. In this research, the charge compensation mechanism of the Gd_2O_3(100)/Si(100) was speculated through the study of these systems.

Silicon is considered to have a non-polar structure which does not exhibit a polar surface. When the (100)-oriented Gd_2O_3 which contains a polar-surface is grown onto the silicon substrate, the polar interface between the two is created due to the polar discontinuity. Thus, the electrostatic potential within the Gd_2O_3 layer as well as the surface energy diverges as a function of thickness unless a charge compensation mechanism takes place. Comparing to the case of LAO/STO, a thickness limit for the Gd_2O_3(100) structure to maintain its stable structure without the charge compensation could be as thin as 2 unit cells or less owing to its high ionicity (figure 11-1,2).

Due to a strong oxygen affinity of the silicon and the strength of Si-O bond, the growth of Gd_2O_3 onto silicon substrate typically terminates with the Gd-O-Si bonding at the interface [45]. This means that the Gd_2O_3 layer is terminated with a negatively charged plane. In order to stabilize the structure according to Eq. 5, the surface/interface layers must be modified such their net charge per unit area is half of the bulk charge per unit area (σ_s).

Considering 6 electrons from $2Gd^{3+}$ for each Gd_2O_3 molecule, the dipole moment and charge per unit area on each plane of the Gd_2O_3(100) can be written as; $\mu_s = 6\sigma_s' d$ and $\sigma_s = \pm 6\sigma_s'$, where $\sigma_s' = e \times number\ of\ Gd_2O_3\ molecule\ per\ unit\ area$. In order to stabilize this structure, the net charge per unit area of the surface/interface region must be modified to $\pm 3\sigma_s'$. The simplest way to obtain such net charge density is to remove oxygen atoms, creating oxygen vacancies. If this type of charge compensation were to take place only on the terminating layer, half of the oxygen atom must be removed as can

be seen in figure 11-c. This is not practical at the Gd_2O_3/Si interface as the localized strain will be high enough to rip the layer off. If more than one layer is involved in this charge compensation mechanism, the amount of oxygen vacancies required can be distributed to the inner oxygen layers. For instance, if three layers of oxygen and two layers of gadolinium are involved in the charge reconfiguration, removal of *1/12* of the oxygen atom per oxygen layer is required in order to obtain the net charge per unit area of $-3\sigma_s'$ and suppress the divergence of the dipole moment as illustrated at the Gd_2O_3/Si interface of the figure 11-d. This mechanism cannot happen if the layer is too thin but not thin enough to be stable. In other words, a thicker layer allows more degree of freedom in lowering the energy of the system as well as complexity.

Furthermore, it can be seen in figure 11-d that when the charge compensation mechanism on the surface is different from the interface, the net dipole moment perpendicular to the surface is not zero but the divergence is suppressed as the net dipole moment no longer depends on the thickness of the layer. It is the charge reconfiguration of the modified region that determines the net dipole moment in this case.

The stabilization of the polar surface can also be described using the bond-transfer model proposed by Noguera [34]. The important fact shared by the two models is that the negative charge per unit area in the surface/interface region must be reduced by half.

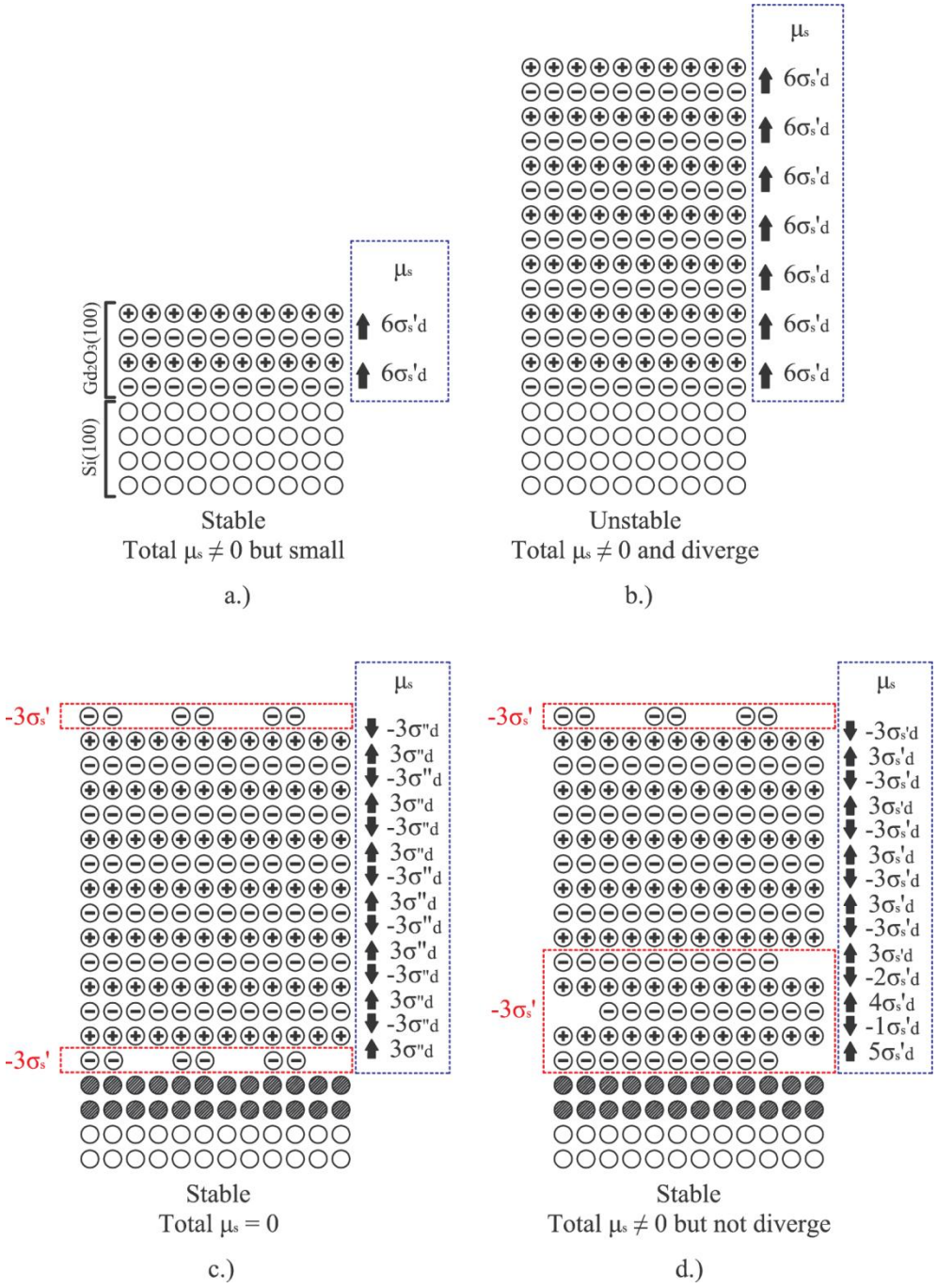

Figure 11. Illustration of the stability of the type III ionic crystal layer grown on a non-polar substrate as a function of thickness and the dipole moment configuration (illustrated to the right of the structure where *d* represents an inter-planar spacing). (a) A stable layer in a thin-limit with non-zero net dipole moment perpendicular to the surface. (b) An unstable layer with a diverging net dipole moment. (c) A stable layer with zero net dipole moment. (d) A stable layer with a constant net dipole moment regardless of the thickness.

2.5 Defect Induced Quantization

Charges can be induced or transferred across the interface through various mechanisms. One of the most well-known mechanisms is through the lining up of the Fermi level of a homojunction, as well as heterojunctions. Another example is the accumulation of charges at the interface due to the difference in macroscopic polarization between two layers of polar semiconductors, e.g. AlGaN/GaN. In the case of the Gd_2O_3(100)/Si(100), the most direct way in maintaining the cubic structure having oxygen vacancies is to transfer extra electrons across the interface to the silicon, which is illustrated as a shaded circle in figure 11-c,d. The mechanism allows the transfer of carrier to silicon, quite similar to transfer doping, with realignment of Fermi level resulting in the creation of occupied quantum states similar to field induced quantization, without the requirement of biasing. As the charge transfer across the interface is governed by the lowering of the interfacial energy, the amount of charge transfer is proportional to the number of oxygen vacancies close to the interface. In thicker layer where the oxygen vacancies spread deeper into the inner part of the layer, a great amount of electrons could be trapped within the Gd_2O_3 layer, resulting in a lower charge transfer. This charge transfer into a semiconductor also gives rise to band bending. As electrons are transferred from the oxide into the silicon, the oxide interface becomes positively charged and its band energy becomes lower. On other hands, the silicon interface becomes negatively charged and the band energy becomes higher. The bending up on the silicon side results in confinement as in field induced 2D confinement. This applies to all type of substrate. However, in the p-type substrate, the transferred electrons is overwhelmed via

recombination with holes, creating a depletion or at most slight inversion layer at the interface shown in figure 12-b. On the other hand, the transferred electrons are accumulated in the conduction band of the n-type and intrinsic substrate, similar to field induced inversion layer of MOSFETs (figure 12-a). A significant increase in mobility is, therefore, attributed by the 2D quantum confinement of electrons transferred from oxygen vacancies within the Gd_2O_3. This phenomenon is exactly what we observed in the measurement of mobility for the transfer of electrons into three types of substrate.

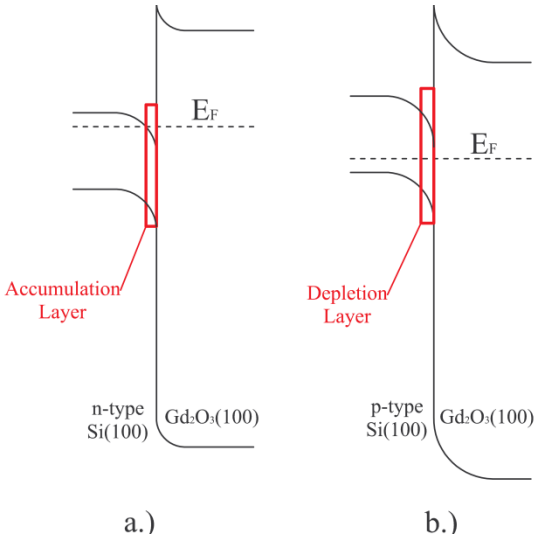

Figure 12. Band diagrams illustrating the accumulation in the conduction band of the n-type silicon (a.) and the compensation in the valence band of the p-type silicon (b.).

CHAPTER 3: EXPERIMENTAL DETAILS

3.1 Growth Procedures

In this research, the growth of Gd_2O_3 is focused on three types of the Si(100) substrate, i.e. intrinsic (280-330 Ω-cm), p-type (1-20 Ω-cm) and n-type (1-10 Ω-cm). The wafers were cleaned by a standard Piranha cleaning procedure, which is a mixed solution between H_2SO_4(96%) and H_2O_2(30%) with 2:3 ratio, for 25 minutes. A native oxide was removed by immersing the wafer in a dilute HF(4.5%) for 30 seconds. The silicon surface was also passivated with hydrogen through this step. Cascade de-ionized water was used for rinsing between each step. The as-cleaned wafers were immediately loaded into the MBE growth chamber with a base pressure in the range of $1\text{-}8x10^{-9}$ Torr. The Gd_2O_3 source includes e-beam with a high purity Gd_2O_3 powder (99.999%). The external oxygen supply is introduced through a mass flow controller unit which is attached with RF plasma generator.

The growth conditions such as growth temperature, oxygen partial pressure and surface reconstruction for different orientations of the Gd_2O_3 were listed in table 3.

Table 3. The growth parameters for different Gd_2O_3 orientations on Si(100)

Orientation	Temperature range (°C)	Oxygen Partial Pressure (Torr)	Surface reconstruction
(111)	100-500	10^{-8}-10^{-6}	Any
(100)	150-200	10^{-7}-10^{-6}	1x1
(110)	600-700	10^{-8}-10^{-7}	2x1

For the growth that requires an unreconstructed surface (1x1), the ramp rate of 10ºC/min was used. It was found experimentally that the higher ramp rate shows a tendency to start the surface reconstruction at a lower temperature. A comparison between the Reflection High-Energy Electron Diffraction (RHEED) pattern of the Si(100) surface at 200ºC with temperature ramp rate of 20ºC/min and 10ºC/min are illustrated in figure 13-a,b, respectively. Faint streaks between the unreconstructed streaks tends to appear earlier with a higher rate as can be seen in figure 13-a. With a higher ramp rate, the surface of the wafer is affected by the increase in the heat output from a substrate heater. It was observed from the RHEED pattern during the temperature ramp that the surface reconstruction starts at 140ºC with the ramp rate of 20ºC while the surface reconstruction starts at 275ºC for the ramp rate of 10ºC. The slow ramp rate also has advantage in preserving the hydrogen passivation. The effectiveness of the hydrogen passivation was tested in a separate set of experiment by intentionally introduce oxygen plasma to the as-cleaned Si(100) wafer at 300°C for 5 minutes. The thickness of the native oxide after the exposure measured by the Filmetrics Thin-Film Analyzer F20 was found to be less than 5 Å, which is much less than a typical native oxide thickness found on bare silicon wafer (25 Å).

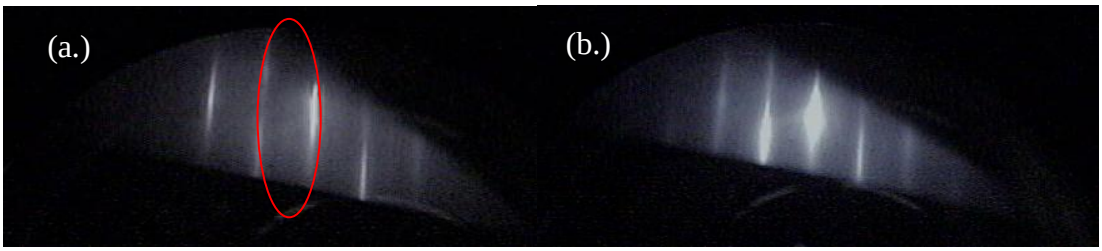

Figure 13. RHEED pattern of the Si(100) surface at 200°C before the growth with the temperature ramp of (a.) 20°C and (b.) 10°C.

The growth of Gd_2O_3(111) on Si(100) is the most feasible growth mode that can occur. It can be obtained with a wide range of growth temperature (100-500˚C) and oxygen partial pressure ($1x10^{-8}$-$1x10^{-6}$ Torr) due to its low surface energy. However, this orientation is an undesirable growth mode as it exhibits the largest lattice mismatch to the Si(100) substrate. In addition, the Gd_2O_3(111) crystallite is one of major components that obstruct the single crystal growth of Gd_2O_3(100) because of the overlapping range of growth parameters between the two. The growth of Gd_2O_3(110), on the other hand, could only be achieved at a higher growth temperature (600-700˚C) with a relatively lower oxygen partial pressure (10^{-8}-10^{-7} Torr).

As for the growth of Gd_2O_3(100), it can only be grown within a very narrow range of temperature 150-200˚C. A lower growth temperature result in a mixture of amorphous and Gd_2O_3(111) structure while a higher growth temperature results in either predominant Gd_2O_3(111) or Gd_2O_3(110). Since the Gd_2O_3(110) structure normally dominates at the growth temperature above 600°C, its contribution at 150-200°C is negligible compare to the Gd_2O_3(111) and Gd_2O_3(100). In order to suppress the formation of the Gd_2O_3(111), the unreconstructed surface is required as the (2x1) reconstructed surface was found to promote the growth of Gd_2O_3(111).

As the Gd_2O_3 source is used repeatedly under the high vacuum, the bombardment of high energy electrons will dissociate the oxygen from the source. Eventually, gadolinium oxide source will change its stoichiometry into the form with lower oxygen content. When this reach the point where the amount of oxygen ions emerging from the source is significantly less than the gadolinium ions, the growth will contains a relatively

thick silicide interfacial layer even at 200°C. As a result, the template for the epitaxial growth is disrupted.

In order to preserve the stoichiometry, external oxygen must be introduced. The introduction of oxygen partial pressure was varied depending on the source condition. For a fresh Gd_2O_3 source, no oxygen partial pressure is needed for growth rates in the range of 0.4-0.6 Å/s. However, after few growths, the source loses a significant amount of oxygen, requiring the introduction of a molecular oxygen partial pressure in the range of 10^{-7}-10^{-6} Torr. This demand in the amount of oxygen partial pressure required increases with the number of growth due to a lower effectiveness of molecular oxygen in replenishing the oxygen deficiency at low temperature. When the required molecular oxygen partial pressure exceed $1x10^{-6}$ Torr, the mean free path of the incoming gadolinium and oxygen ions will be significantly reduced and the growth rate becomes excessively low. Furthermore, the high oxygen partial pressure will also damage or reduce the lifetime of many components in the MBE chamber such as the filament for the electron beam and the effusion cell, as well as a cryogenic pump. Thus, the molecular oxygen must be replaced with oxygen plasma. In addition, the surface must also be exposed to the oxygen plasma for up to 10 seconds before the introduction of the Gd_2O_3 source. The oxygen plasma used in this experiment was generated using RF plasma generator with the forward power of 200 Watts.

It should be noted here that the oxygen plasma is one of possible solutions. However, the ions from plasma are very reactive and contain a considerable amount of kinetic energy. Thus, the growth using oxygen plasma tends to contain point defects. Furthermore, due to its high kinetic energy and reactivity, a thick oxygen-rich interfacial

layer could easily be formed and the growth of Gd_2O_3(100) will no longer be possible. Therefore, the growth of the Gd_2O_3(100) requires a precise control over the introduction of the source in order to prevent the formation of such interface layer.

As the generation of the oxygen vacancies becomes significant at high growth temperature, this low growth temperature not only ensures the reduction of oxygen vacancy density but also localizes them close to the surface/interface [65-67]. The inter-diffusion which is the cause of the formation of interfacial layer was also minimized through this low growth temperature and the hydrogen passivation. This growth represents a modification from the method of growing CeO_2(100) on Si(100) [68].

The thickness of the sample in this research ranges from 5-150 nm. This short growth time, 15-45 minutes, has advantage in term of minimizing the variation from the Gd_2O_3 source condition during the growth.

3.2 Sample Processing

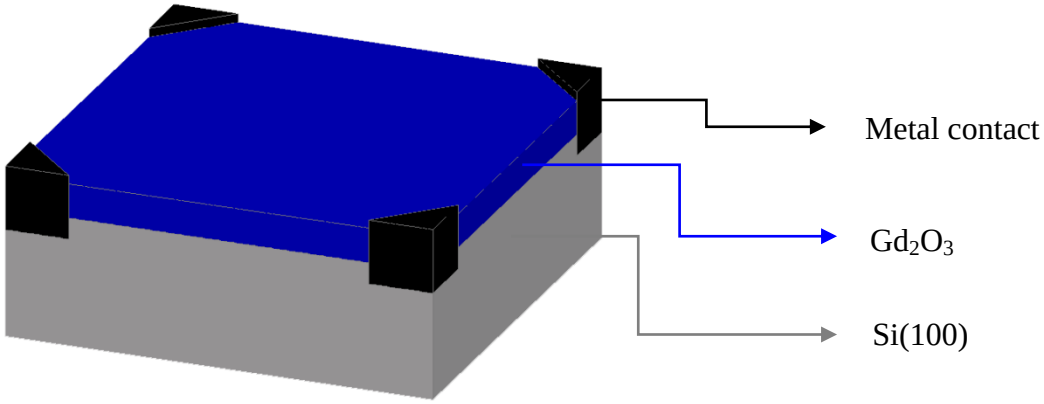

Figure 14. Van der Pauw configuration for Hall measurement

After the crystal structure was characterized by x-ray diffraction (XRD) technique, a van der Pauw contact configuration was made according to the widely accepted configuration for measuring the carrier mobility and I-V characteristic (figure 14) [69]. As an ohmic contact is required for a Hall mobility measurement, aluminum was selected as a metal contact for all types of silicon substrate. The aluminum is known to form an ohmic contact with p-type silicon substrate but a Schottky contact with a lightly doped n-type silicon substrate. However, the width of the Schottky barrier can be narrowed down by the high electron concentration in the accumulation region close to the interface. If the barrier width is thin enough, electrons can tunnel through the Schottky barrier, thus, exhibiting a tunneling ohmic contact characteristic. Other metals, such as $In_{0.95}Sn_{0.05}$ and high purity silver pasted were also used as an alternative ohmic contact for the sample that did not exhibit the electron accumulation at the interface.

In order to deposit the front contact onto the silicon substrate, the Gd_2O_3 layer was etched with a dilute H_2SO_4(4.5%) to create a *via*. Then, the exposed silicon was slightly etched (~100 nm-deep) using SF_6 in Reactive Ion Etching (RIE). This step is performed in order to increase the contact area between the accumulation layer, if any, and metal. Different metals were deposited with different technique and anneal at different temperature as illustrated in table 4. Finally, the samples were diced into a smaller piece with a dimension of 1x1 cm^2.

Table 4. A list of deposition techniques and annealing temperature/time for different metal contacts.

Metals	**Deposition**	**Annealing Temperature/time**
Aluminum	Sputtered	475˚C/10 min
Silver paste	Painted	200˚C/10min
$In_{0.95}Sn_{0.05}$	Soldered	200˚C/10min

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Structural Characterization

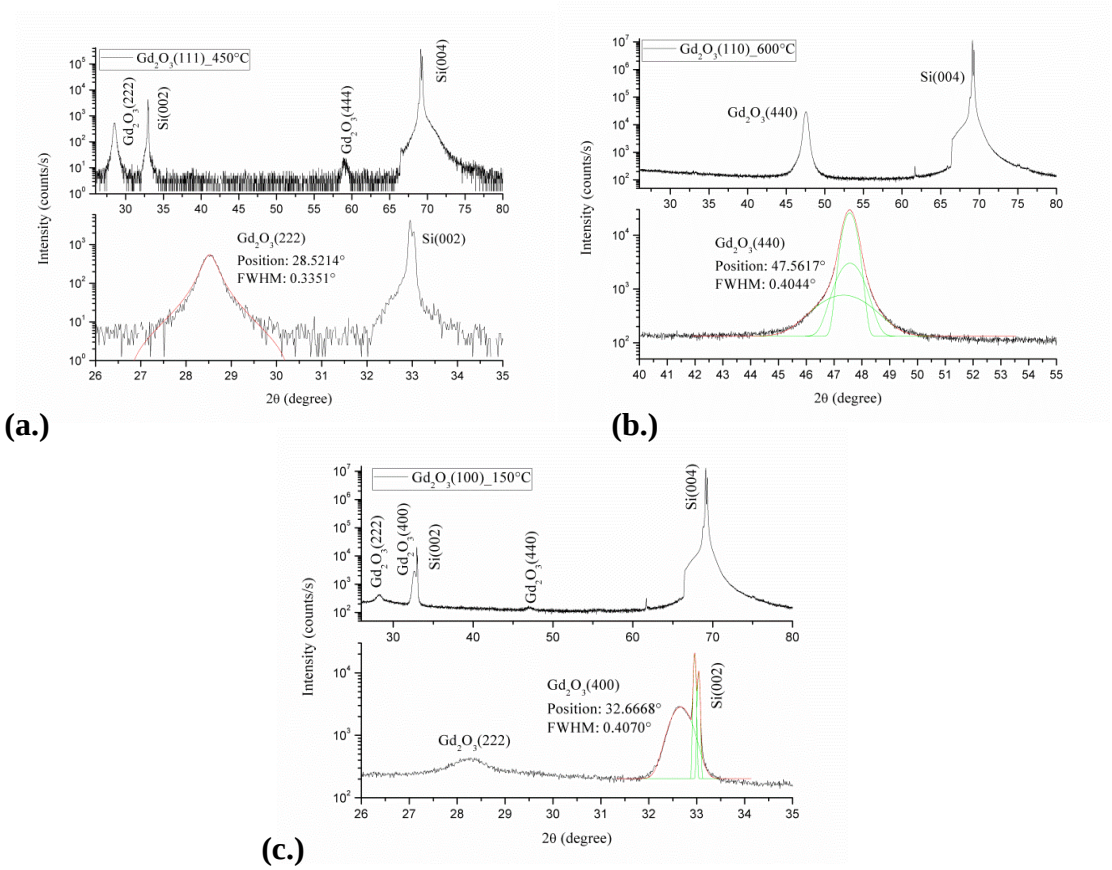

Figure 15. XRD patterns of three possible growth mode of the Gd_2O_3 on Si(100) grown at (a.) 150°C, (b.) 600°C and (c.) 450°C

Structure of the grown samples were characterized using the x-ray diffraction (XRD) from X-ray Diffraction System X'Pert Pro MRD while the thickness was measured using FilMetric F20 Thin-Film Analyzer. Figure 15 illustrates the effect of growth temperature on the growth mode through the XRD pattern of three samples grown

at different substrate temperature. As discussed in the previous chapter, the (111)-oriented Gd_2O_3 can be obtained within the range of 100-500°C as illustrated in figure 15-a. When the growth temperature reaches 600°C, the (110)-oriented Gd_2O_3 can be formed with a proper oxygen partial pressure (figure 15-b). As for the sample with Gd_2O_3(100) structure (figure 15-c), they could only be obtained when the growth temperature is between 150°C and 200°C. A single crystal Gd_2O_3(111) and Gd_2O_3(110) can be obtained rather easily unlike the growth of the Gd_2O_3(100) as can be seen in the XRD patterns. The reason behind the polycrystalline structure of the Gd_2O_3(100) could be attributed to its high defect density which results from the energy lowering mechanism as discussed in chapter 2.

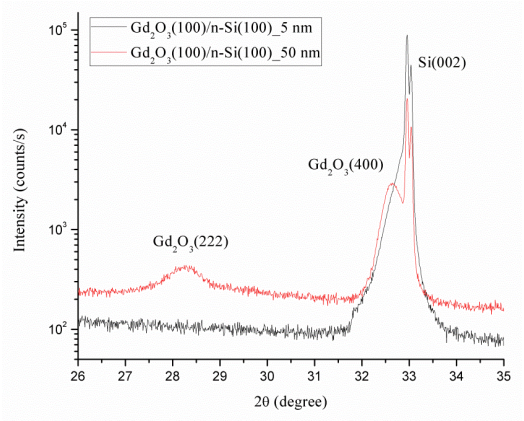

Figure 16. XRD pattern of the growths on n-type Si(100) comparing a single crystal Gd_2O_3(100) and the polycrystal with a predominant Gd_2O_3(100) structure. The thicknesses for each sample are 5 and 50 nm, respectively.

Due to its polar surface properties, a single crystal Gd_2O_3(100) could only be found when the deposited layer is sufficiently thin (figure 16). When thickness as well as a stored energy exceeds a critical value, the defects are generated, in particular at the surface/interface, from charge compensation mechanism. This high density of oxygen vacancy near the surface may serve to disrupt the Gd_2O_3(100) template for a subsequent

growth. In other words, the structure will be composed of the layer of $Gd_2O_3(100)$ next to the Si/Gd_2O_3 interface and the polycrystalline Gd_2O_3 close to the surface.

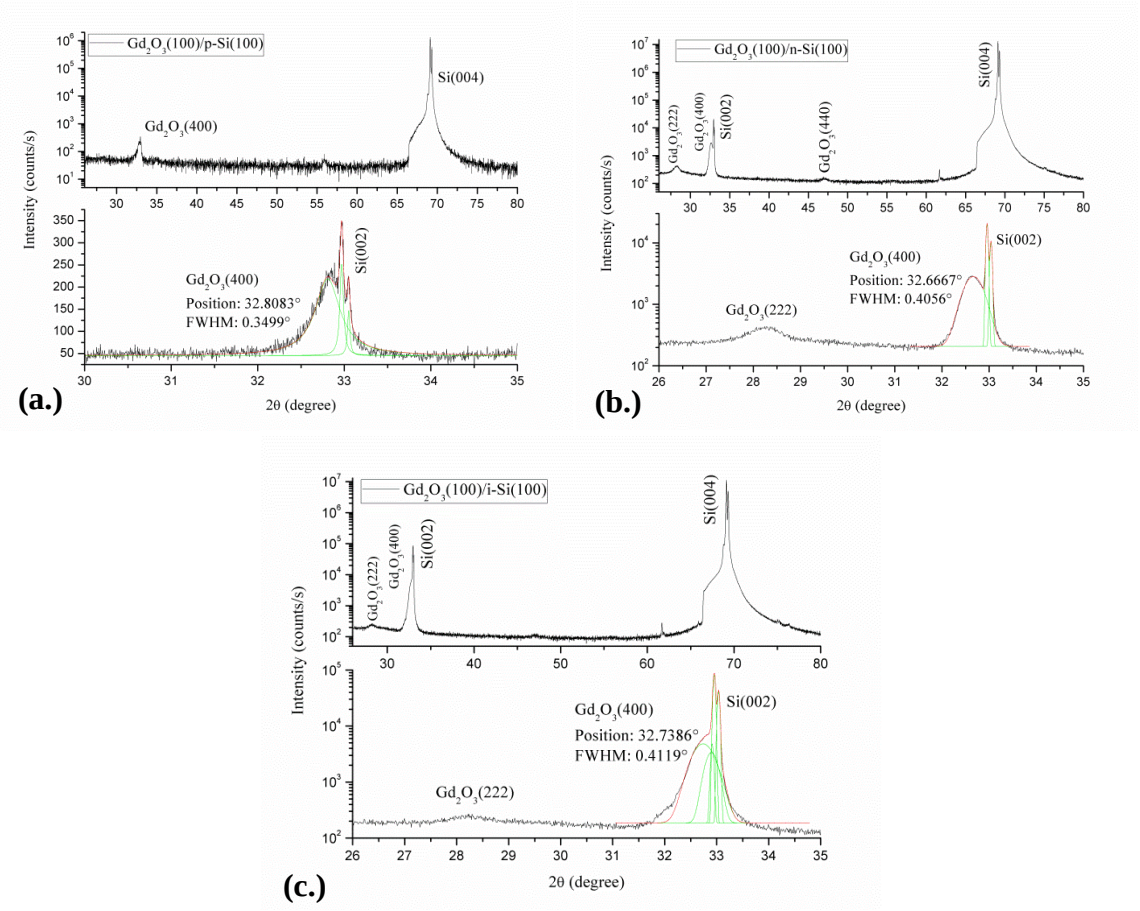

Figure 17. XRD patterns showing different structure obtained from different substrate. a.) p-type Si(100), b.) n-type Si(100), c.) intrinsic Si(100)

Different substrate types also affect the stabilization of the $Gd_2O_3(100)$ structure differently. Figure 17 shows different crystallinity of the $Gd_2O_3(100)$ grown on three types of Si(100) wafer. A 150 nm-thick single crystal $Gd_2O_3(100)$ was grown on the p-type substrate (figure 17-a) while a 50 nm and 30 nm-thick polycrystal were grown on the n-type (figure 17-b) and intrinsic (figure 17-c) substrate, respectively. It was found that the $Gd_2O_3(100)$ grown on p-type substrate exhibits the best structural consideration

from XRD. The terrace/grain size of the Gd_2O_3(100) on p-type, n-type and intrinsic substrate calculated using Scherrer formula are 24.75 nm, 21.34 nm and 21.02 nm, respectively [70]. Furthermore, the single crystal Gd_2O_3(100) on the p-type substrate can also be achieved with a thicker layer (>100 nm) compare to n-type and intrinsic substrate. This means that the p-type substrate is superior in terms of stabilizing the polar surface of the Gd_2O_3(100) and lowering the defect density required. It should be noted that the Gd_2O_3(100) is under a tensile strained in the direction perpendicular to the surface as the peak is shifted to the lower 2θ angle. When the sample is annealed in the furnace at 800°C with nitrogen ambient for 15 minutes, the strain is relaxed and the peak shifted back to its original position as shown figure 18.

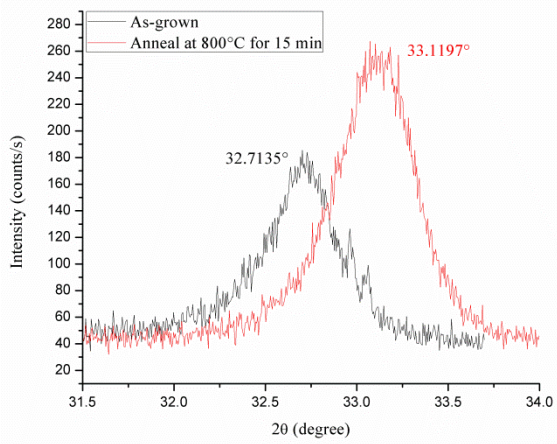

Figure 18. XRD pattern illustrating the strain relaxation of the 150nm-thick Gd_2O_3(100) grown on p-type Si(100) after the annealing at 800°C for 15 min

The growth on n-type and intrinsic substrate, on the other hand, are inferior in term of structural stability. A rather thin Gd_2O_3 layer of 5 nm is required in order to obtain the single crystal Gd_2O_3(100) on n-type Si(100). As for the intrinsic substrate, the growth exhibits a room temperature instability which can be observed from the disappearance of the Gd_2O_3(400) peak over a span of 19 hours as shown in figure 19-a.

The decrease in the forbidden Si(002) peak also indicates the change of structure involving interface region. Our results support the model for a more stable structure requiring a higher density of oxygen vacancy which, apparently, introduce the formation of other orientations including Gd_2O_3(111) (figure 19-b).

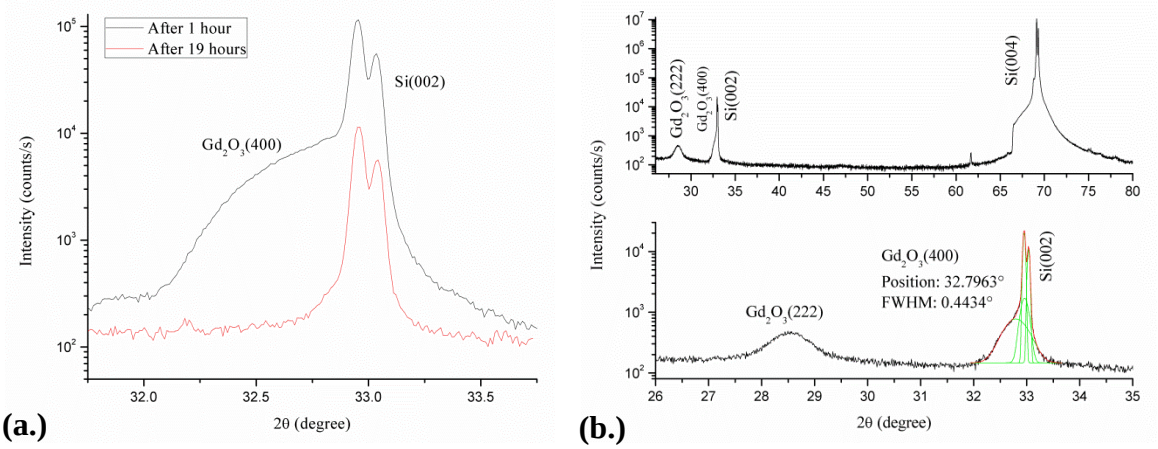

Figure 19. XRD pattern illustrating (a) the instability of the 30 nm-thicked Gd_2O_3(100) grown on the intrinsic Si(100) substrate through the disappearance of the Gd_2O_3(400) peak over a course of 19 hours, and (b) a stable Gd_2O_3(100) on i-Si(100) with a lower crystalline quality.

The growth of the Gd_2O_3(100) not only depends strongly on the growth parameters such as growth temperature and substrate type, but also oxygen partial pressure and surface preparation. One of major problems arises from the lack of oxygen is a formation of silicide (Gd_xSi_y) interfacial layer. At approximately the same oxygen deficiency level in the source, the formation of the silicide was found to be a function of temperature. For a relatively fresh source, the Gd_2O_3 layer can be grown without the formation of the silicide observable in the XRD up until 450°C. Above 600°C, a thick silicide layer can be observed. With a thick silicide layer, it is no longer possible to grow a single crystal Gd_2O_3(110) like the sample in figure 15-b as the template for the epitaxial

growth has been disrupted. It should be noted that, with a higher degree of oxygen deficiency, the formation of silicide could start at the temperature as low as 175°C. When that happen, the silicide could obstruct the growth of the Gd_2O_3(100) the same way as it obstruct Gd_2O_3(110) growth.

At high temperature, this problem can be easily solved by introducing external molecular oxygen into the chamber. However, at the temperature of 200˚C, the oxygen molecule is much less reactive than at 600˚C, requiring a higher amount of oxygen supply. As the source continues to lose oxygen, the amount of oxygen partial pressure required changed more abruptly than the growth at high temperature. Because of this, providing the right amount of oxygen partial pressure turns out to be quite challenging. An insufficient amount of oxygen partial pressure cannot suppress the formation of silicide while excess oxygen partial pressure will turn the structure into an amorphous layer. The appropriate amount of the oxygen partial pressure for the low growth temperature could vary from 10^{-7} Torr to more than 10^{-6} Torr. Even if the right amount of oxygen partial pressure is obtained, the growth of Gd_2O_3(100) will be formed only if two other parameters, which are the growth temperature and the sequence of source introduction, are adjusted accordingly. Fortunately, the last two parameters do not fluctuate as much as the oxygen partial pressure. Thus, the loss of oxygen from the source is a major problem for the growth of the Gd_2O_3(100).

As discussed earlier, the growth temperature could also be used as a mean to suppress the formation of the silicide. The samples in figure 20 were grown when the oxygen in the source was highly depleted. In this case, oxygen plasma was used instead of the molecular oxygen. The oxygen partial pressure was in the range of $8x10^{-7}$ Torr and

the unreconstructed surface was exposed to oxygen plasma for up to 10 seconds before the introduction of the Gd_2O_3 source. With the same oxygen partial pressure and the source introduction sequence, the sample grown at lower temperature exhibits a lower Gd_2O_3(222) peak and no GdSi(111) peak while maintaining almost the same Gd_2O_3(100) structure.

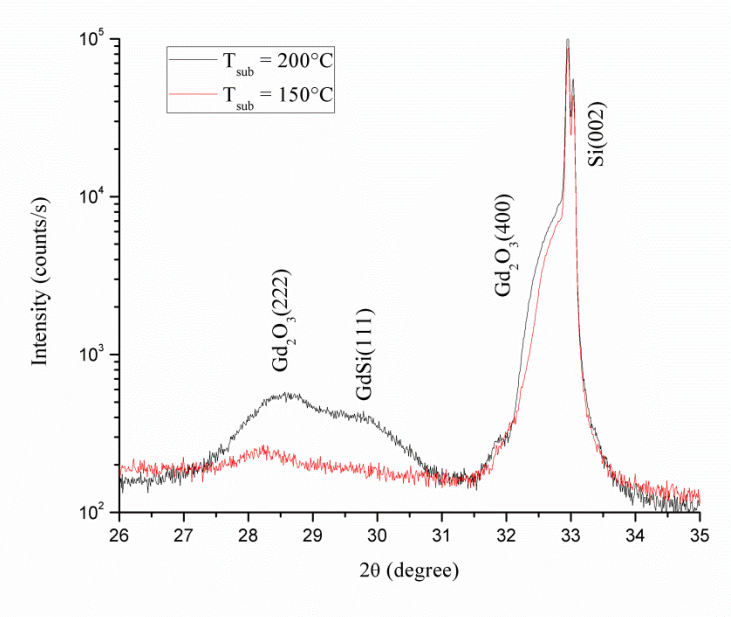

Figure 20. XRD patterns of the polycrystal with predominant Gd_2O_3(100) structure grown on the intrinsic Si(100) illustrating the suppression of the silicide formation through a low growth temperature.

In most case, the formation of silicide and Gd_2O_3(100) were not observed together as they are the structure that takes place mainly at the interface. The coexistence of the Gd_2O_3(100) and the silicide signifies a sharing of Si(100) surface occupancy with the Gd_2O_3(100) as a predominant structure.

As a direct growth of the Gd_2O_3(100) on Si(100) is relatively hard to obtain due to the growth parameters that change too quickly over time, attempts have been made on an alternative approach. In this approach, the growth was done by low temperature

deposition follow by a high temperature annealing. The sample with the amorphous Gd_2O_3 deposited at 80°C was annealed at 475°C, 600°C and 1000°C for 10 minutes, 15 minutes and 5 minutes, respectively. The annealing at 475°C and 600°C results in a weak Gd_2O_3(111) crystallization, while the annealing at 1000°C results in the formation of silicide and the change of phase from cubic into monoclinic.

From these results, the Gd_2O_3(100) cannot be obtained just by annealing an amorphous Gd_2O_3 layer since there is no constraint to stop the layer from assuming the structure with lowest surface energy, i.e. Gd_2O_3(111). However, if the Gd_2O_3 layer contains a significant amount of Gd_2O_3(100) crystallites as can be seen in figure 21, the rapid thermal annealing (RTA) could greatly enhanced the crystallization of the Gd_2O_3(100).

As the heat source of the Rapid Thermal Processor is a high intensity Tungsten Halogen Lamp which has the peak intensity in the visible range close to infrared, majority of the light will not be absorbed by the Gd_2O_3 layer which has a bandgap of 5.8 eV. As a result, the silicon substrate, as well as the interface region, will be heated up first. Because of this heat gradient, the Gd_2O_3(100) crystallites which lie next to the interface act like a seed for crystallization. A very similar intensity of the Gd_2O_3(400) peak from different location of the same sample confirms the uniformity of the Gd_2O_3(100) layer next to the interface. The major advantage of this method is a higher repeatability since it is not required that the Gd_2O_3(100) be a predominant structure. As for the disadvantages, this method introduces undesirable structures and interfacial layer which exhibit nonuniformity across the sample.

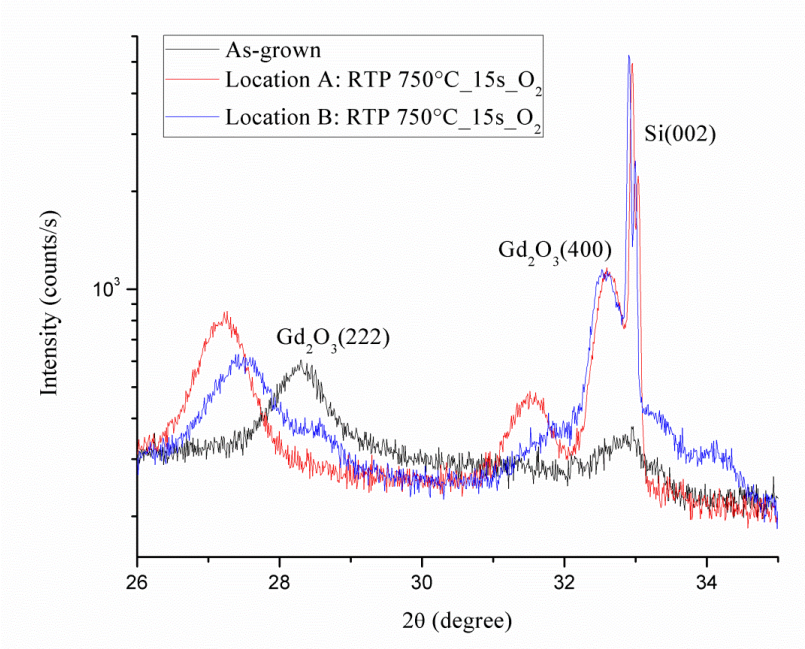

Figure 21. XRD patterns of the 60 nm-thicked Gd_2O_3 deposited on n-type Si(100) at 175°C, before and after RTA at different location.

For a comparison purpose, the Gd_2O_3 was deposited using an oxygen deficient source on a fused silica substrate at 200°C as can be seen in figure 22. Even with the oxygen-rich fused silica, the majority of the structure was found to be silicides. After the sample were annealed at 600°C for 10 minutes in furnace with N_2 ambient, the stoichiometry of the silicide was changed and the Gd_2O_3 structures were recovered to some extent. The powder diffraction files for indicating diffraction peaks can be found in appendix B.

Presently, we have identified some adverse effect caused by inadvertent formation of silicide in the growth of the Gd_2O_3(100) on Si(100). It will be shown in the next section that the presence of silicide can be correlated to the inferior mobility enhancement. As for a better stability of the Gd_2O_3(100) on n-type and p-type substrate compare to the intrinsic substrate, it could be attributed to a better lattice match which

arise from a contraction in the lattice parameter of the boron-doped silicon substrate [71]. In addition, the local fluctuation of the polar surface may be smoothed out by the conducting charges [34, 35]. Therefore, the superior stability of the Gd_2O_3(100) on n-type and p-type may also be attributed to the same reason where the dipole at the interface is smoothed out by the free carrier. Although the understanding in this area requires further investigation, the lightly doped n-type silicon we used provides more than sufficient improvement for epitaxial growth of Gd_2O_3(100) on Si(100).

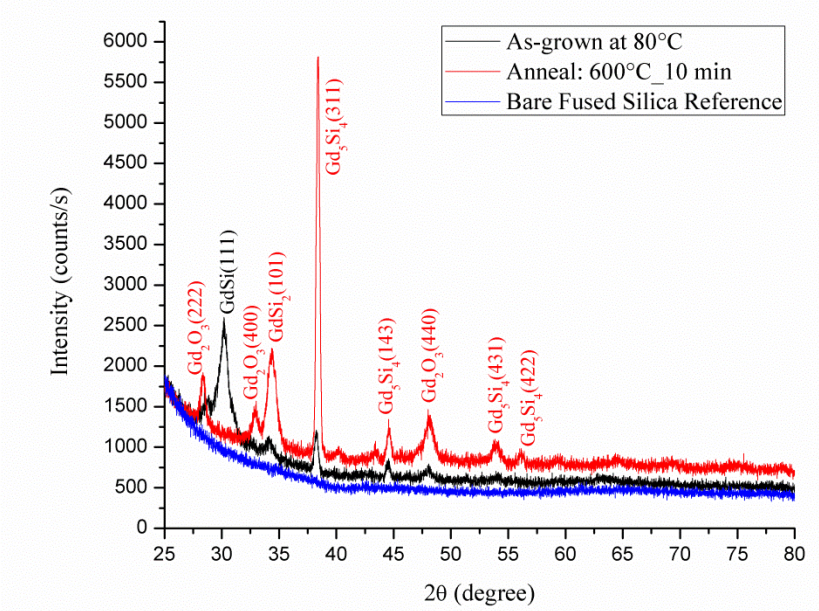

Figure 22. XRD patterns of an 80 nm-thick Gd_2O_3 deposited on fused silica substrate at 200°C before and after annealing in furnace with N_2 ambient

4.2 Electrical Characterization

High-κ dielectric is known to degrade carrier mobility mainly through the remote phonon and Coulomb scattering [38]. However, as the remote Coulomb scattering can be screened by a high carrier density at the interface, higher electron mobility was observed at the Gd_2O_3(100)/Si(100) interface due to accumulation of the transferred electrons and quantum confinement at the interface. The room temperature carrier mobility and sheet carrier concentration as well as an IV characteristic were measured using Hall Effect Measurement System (HMS-3000) and Kiethley SCS4200.

A summarize of the carrier mobility at different doping concentration of a bulk silicon at 300 K can be seen in figure 23. The doping concentration for the n-type and p-type substrate used in this research are in the range of $5x10^{14}$-$5x10^{15}$ cm^{-3} and $7x10^{14}$-$1x10^{16}$ cm^{-3}, respectively. Thus, the expected maximum mobility for a bulk substrate is 1382 cm^2/Vs for electrons and 464 cm^2/Vs for holes.

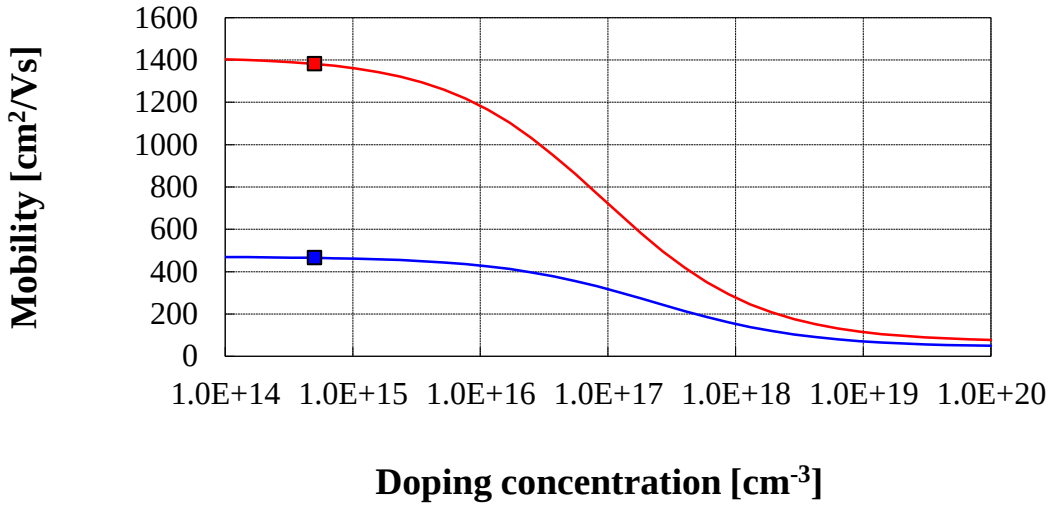

Figure. 23 Variation of carrier mobility in bulk silicon at 300K with doping concentration

In order to verify the ohmic contact of the sample, the IV characteristic between the four contacts was tested before the Hall mobility is measured. Figure 24-a, b illustrate the ohmic contact characteristic from the sample with p-type and n-type substrate, respectively. It can be seen that the aluminum contacts on p-type substrate exhibit a better ohmic contact characteristic than n-type substrate. However, the fact that the aluminum contact exhibits the ohmic characteristic with a lightly doped n-type substrate indicates an increase in carrier mobility within the silicon, thus, confirming the charge transfer from the Gd_2O_3(100) into the silicon.

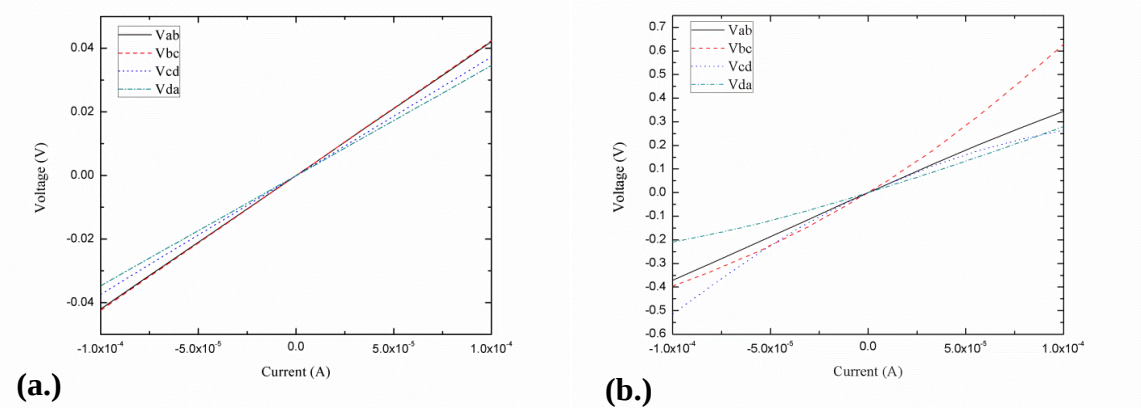

Figure 24. IV curve showing an ohmic characteristic between the four Al contacts on (a.) p-type and (b.) n-type substrate

Figure 25-c and 25-a illustrate the interface band diagrams between two contacts with and without the charge transfer from the Gd_2O_3 into the Si, respectively. The Schottky barrier between the Al and n-type silicon is 0.72 eV as calculated from C-V measurement. With a higher electron concentration from the charge transfer, the depletion width at the Schottky junction is narrowed down, $W_2<W_1$. When the bias is applied between the two electrodes, the thermionic-field emission current through the Schottky barrier of the band with charge transfer (figure 25-d) will be higher than the

band without the charge transfer (figure 25-b). As a result, the I-V characteristic is ohmic for the sample with Gd_2O_3(100) while I-V characteristic of the sample with non-polar surface orientation, such as Gd_2O_3(110) or Gd_2O_3(111), is closer to the Schottky contact.

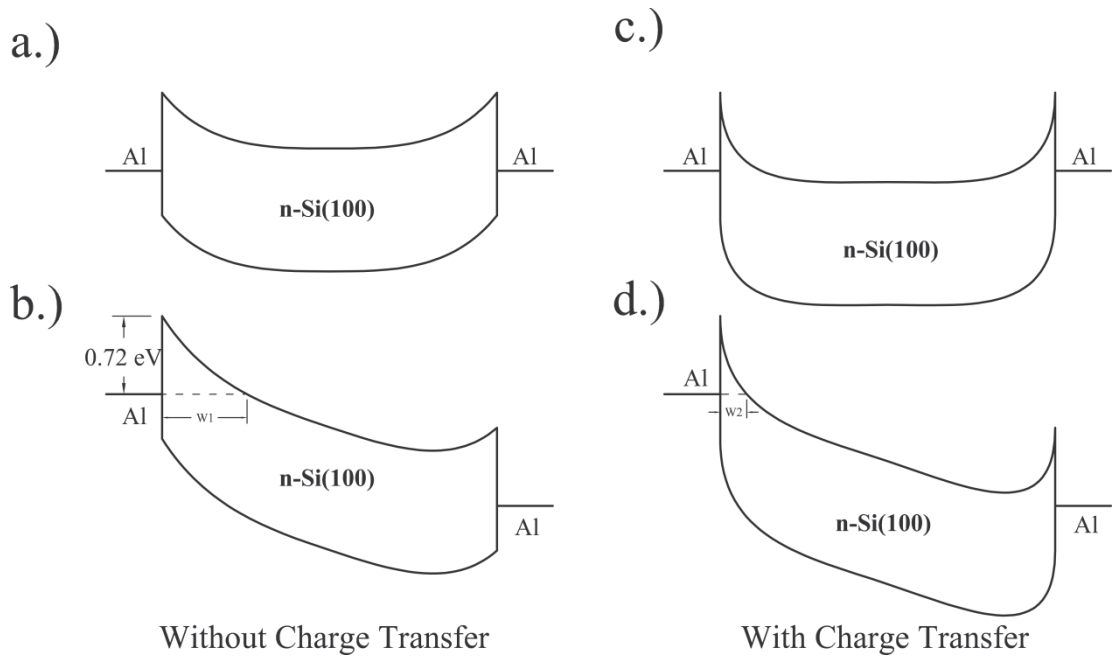

Figure 25. Interface Band diagrams between two Al contacts without the charge transfer (a, b) and with the charge transfer (c, d) at equilibrium and with applied bias.

Figure 26 shows two possible current paths between two contacts. For the sample with Gd_2O_3(100), the band diagram along the path A would be the same as figure 25-d because this path pass through the electron accumulation region. On the other hand, the band diagram along the path B would look similar to the figure 25-b as there is no charge accumulation. If the difference in the depletion width is substantial, the current passing through the path B should be much less than the path A and the mobility and carrier concentration can be selectively probed. However, the position of the Fermi pinning at the aluminum/n-type Si contact is relatively close to the valence band of the silicon.

Therefore, the depletion width from lining up of the Fermi level is almost thin enough for a significant current to tunnel through. Thus, the difference between the two paths is not quite significant. Further improvement in lowering the stray current can be achieved by using the intrinsic Si(100) wafer together with a better metal contact with a proper Schottky barrier height, e.g. ErSi.

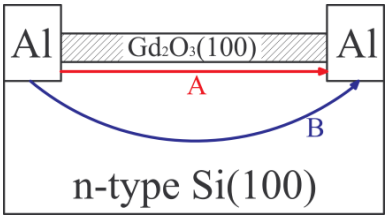

Figure 26. Schematic diagram showing possible conduction paths between two electrodes

As there is no hole for the transferred electrons to recombine with, the intrinsic silicon also exhibit the accumulation of electrons at the interface with improved enhancement of electron mobility. The greatest advantage of the intrinsic silicon is its high resistivity, 300-15,000 Ω-cm. With this, the electron transport will mostly be concentrated within an accumulation region. Thus, the stray current will be reduced. Because of these reasons, the intrinsic silicon substrate becomes the best candidate for selectively probe the carrier mobility and concentration at the interface. Unfortunately, the growth of the high quality Gd_2O_3(100) on the intrinsic substrate suffer from the instability and the Hall measurement can only be made on the stable sample which exhibits a high degree of polycrystallinity.

Hall mobility measurement at room temperature from the sample with a single crystal Gd_2O_3(100) grown on p-type and n-type substrate are shown in figure 27-a,b. The hole mobility measured from the sample with p-type substrate shows a degradation (310-

380 cm^2/Vs) while electron mobility measured from the sample with n-type substrate exhibits an enhancement (1760-1780 cm^2/Vs) with a sheet carrier concentration of 3.4-3.6x10^{13} cm^{-2}. The effective carrier concentration is almost semi metallic (~10^{19} cm^{-3}), yet a higher mobility is obtained. Compared to a heavily doped silicon substrate (figure 23), this would amount to enhancement of electron mobility by a factor of four to five.

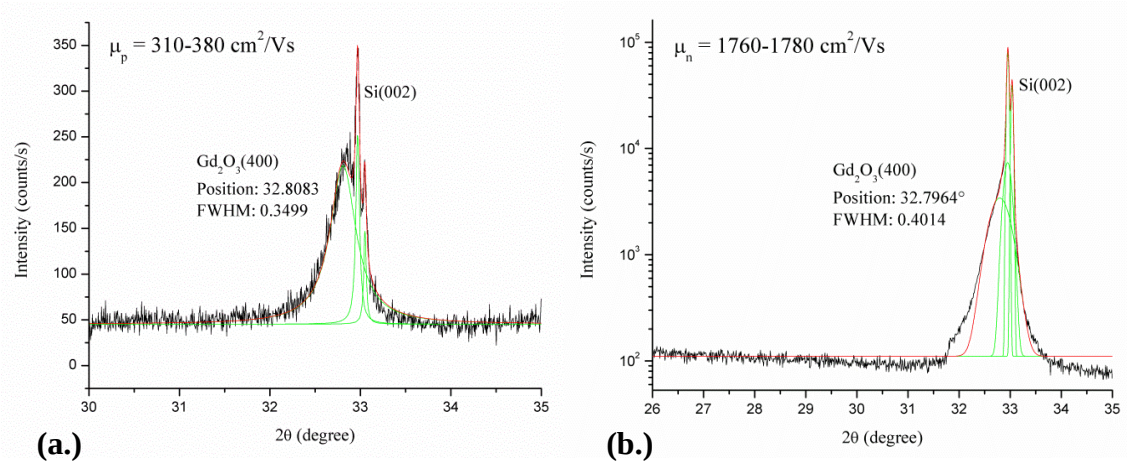

Figure 27. Hall mobility measurement of the single crystal Gd_2O_3(100) grown on (a.) p-type and (b.) n-type Si(100)

The effects of the structural consideration from XRD on the mobility are shown in figure 28. The sample with the Gd_2O_3(100) as a predominant structure (figure 28-a) exhibits a higher electron mobility and carrier concentration than the sample with Gd_2O_3(111) as a predominant structure. As the defective structure provide additional scattering, the mobility from both sample are inferior to the sample with single crystal Gd_2O_3(100). However, their carrier concentration is higher than the single crystal sample. This could be attributed to higher density of oxygen vacancy due to the presence of grain boundary within the polycrystalline structure.

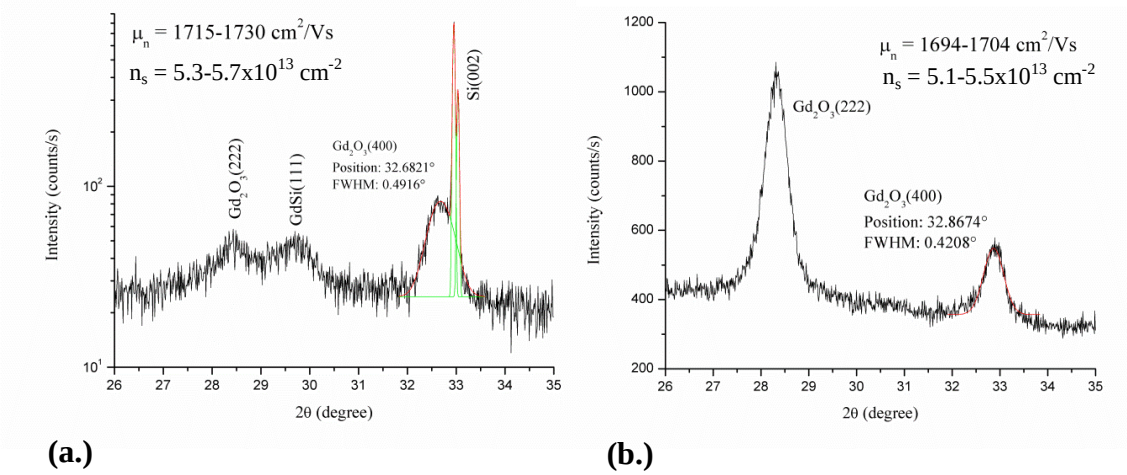

Figure 28. Degradation of Hall mobility due to different structural composition of the (a.) 90-nm and (b.) 80-nm thick polycrystalline Gd_2O_3 grown on the n-type substrate

The mobility of the sample that was annealed using the RTA is shown in figure 29. Even with the presence of undesirable structures, the mobility was found to be as high as 1752 cm^2/Vs because of a high quality $Gd_2O_3(100)$ structure. Though, this mobility is still inferior to the single crystal sample due to its polycrystalline nature.

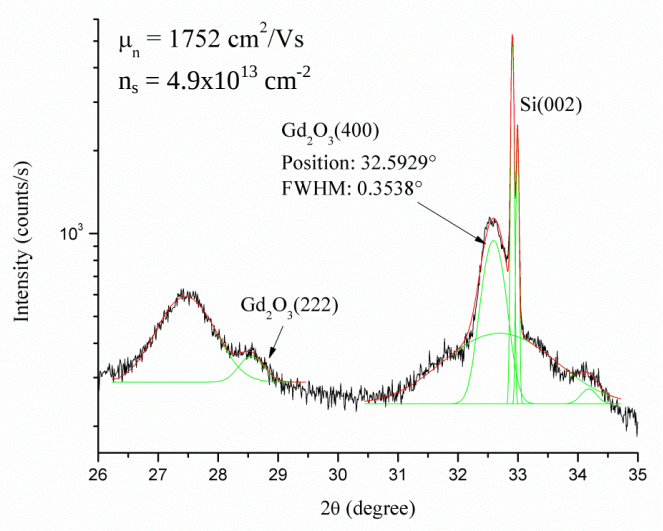

Figure 29. Hall mobility measurement of the RTA-assisted, 58 nm-thick polycrystalline layer with a predominant $Gd_2O_3(100)$ grown on n-type Si(100)

Figure 30 illustrate a study on the effect of amorphous silicon capping layer. When the Gd_2O_3(100) is capped with the amorphous silicon, the Gd_2O_3(400) peak shifts to the higher 2θ angle indicating a compressive strain in the direction perpendicular to the surface. In this case, the inter-planar spacing in the direction perpendicular to the surface was reduced in order to lower the macroscopic dipole moment in that direction. This stabilization involves larger portion of the Gd_2O_3 layer than the case with oxygen vacancies which involves few layers near the surface. This mechanism in lowering the energy of the system arises from a lower degree of freedom in reconfiguring the charges at the surface due to the encapsulation of the silicon on both sides. Although the stabilization of the Gd_2O_3(100) structure with the aid from compressive strain results in a higher charge transfer across the interface, a significant degradation of the crystalline structure due to a non-uniform strain can be observed together with the reduction in electron mobility compare to the case of single crystal growth.

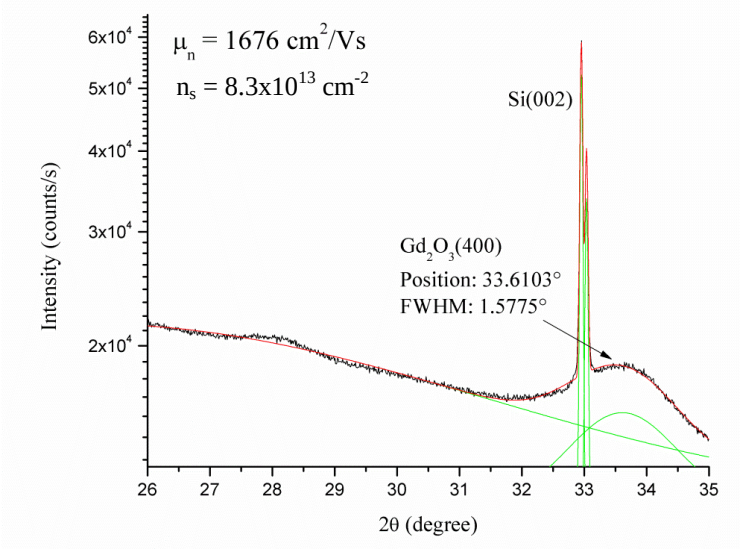

Figure 30. Hall mobility measurement of the 30 nm-thick poly crystal with a predominant Gd_2O_3(100) grown on n-type Si(100) with the amorphous silicon capping layer (50 nm)

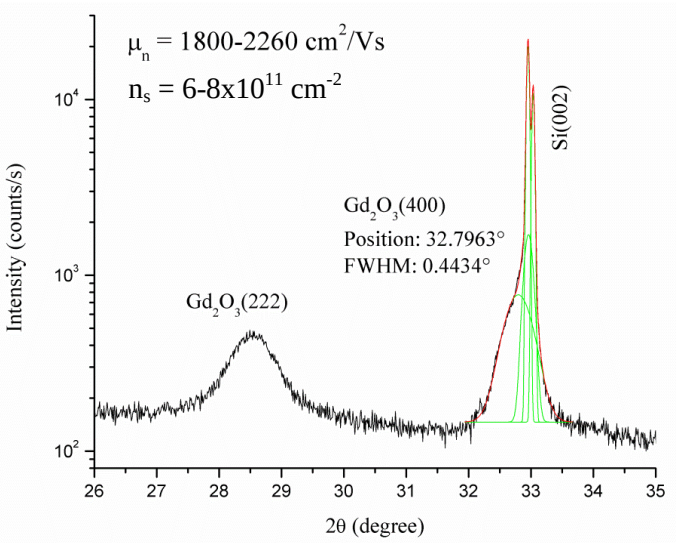

Figure 31. Hall mobility measurement of the polycrystalline with predominant Gd_2O_3(100) grown on intrinsic Si(100)

The Hall mobility measurement of the sample with stable Gd_2O_3(100) grown on intrinsic Si(100) substrate is shown in figure 31. The electron mobility of 1800-2260 cm^2/Vs was found together with the minimum sheet carrier concentration of $6x10^{11}$ cm^{-2} ($> 10^{16}$ cm^{-3}). In spite of a lower charge density, the highest mobility was obtained with the intrinsic substrate due to a lower impurity scattering within the intrinsic substrate. In spite of having desirable electrical properties, the structural instability of the Gd_2O_3(100) on intrinsic substrate render it unsuitable for CMOS applications.

The Hall mobility measurement of Gd_2O_3(110) grown on n-type Si(100) with the XRD pattern shown in figure 32 was also performed for comparison purpose. From the polar surface point of view, the Gd_2O_3(110) surface is considered to be non-polar. Thus, there should be no charge reconfiguration as in the case of the Gd_2O_3(100). However, the measured Hall mobility and sheet carrier concentration was found to be in the range of 1688-1722 $cm^2/V{\cdot}s$ and $5.0\text{-}5.2x10^{13}$ cm^{-2}, respectively. These results are similar to the sample with Gd_2O_3(100). The IV characteristic also shows a decent ohmic contact

characteristic as can be seen in figure 33. With a closer observation, there is an evidence of a small Gd_2O_3(400) peak (figure 32-b). Thus, the small Gd_2O_3(100) crystallites located near the interface could be the cause of this enhancement in carrier mobility.

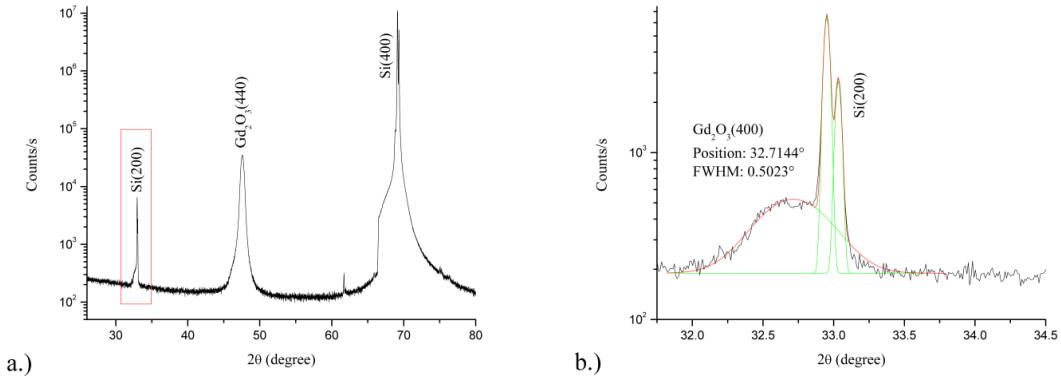

Figure 32. XRD pattern illustrating the polycrystalline structure with Gd_2O_3(110) and Gd_2O_3(100) grown on n-type Si(100). a.) Full scan, b.) Enlargement of the red box

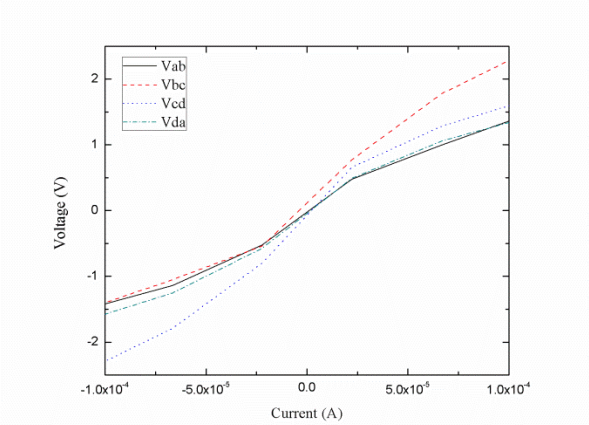

Figure 33. IV curve showing a decent ohmic characteristic between the four Al contacts on n-type substrate with the Gd_2O_3(110) deposited on top

It can be seen from these characterizations that the mobility measurements coincide with the structural consideration from XRD data. However, a definite conclusion regarding the correlation between the carrier concentration and structural characterization still opens up for further investigation.

CHAPTER 5: CONCLUSION

A gadolinium oxide (Gd_2O_3) is a high-κ dielectric known for its potential to replace SiO_2 in MOSFET applications. Its main traits are a lattice match within 0.5% to twice of the silicon unit cell as well as a proper band-edge alignment and thermodynamic stability with silicon. Among the three low index orientation of the Gd_2O_3, only the Gd_2O_3(111) and Gd_2O_3(110) were reported to grow epitaxially on the Si(111) and Si(100) substrate, respectively. The growth of the Gd_2O_3(110) on Si(100) is more favorable than the Gd_2O_3(100) due to its lower surface energy and alternative lattice matching. However, a substantial enhancement in electron mobility can only be found at the Gd_2O_3(100)/Si(100) interface, providing a better performance in term of a lower drive voltage with higher current and faster speed.

The Gd_2O_3(100) samples were fabricated by MBE with the growth temperature and oxygen partial pressure in the range of 150-200˚C and $1x10^{-7}$-$1x10^{-6}$ Torr, respectively. Key to the successful growth of the Gd_2O_3 is the control of oxygen stoichiometry. The repeated use of the source gives rise to the non-stoichiometry of the Gd_2O_3 which needs to be replenished by external oxygen. Satisfactory Gd_2O_3(100) on Si(100) has been achieved with the aid of control of oxygen partial pressure as well as rapid thermal annealing.

When the Gd_2O_3(100), which exhibits a polar surface, is grown onto the nonpolar structure such as silicon, the ordered oxygen vacancies are created at the interface/surface

as a mean to lower the dipole energy with a subsequent of transferring electrons into the silicon. Therefore, silicon has acquired electrons without doping, similar to field-induced inversion layer of MOSFETs. If the silicon is intrinsic or n-doped, extra electrons go into conduction band. However, if the silicon is p-doped, the transfer electrons is overwhelm via recombination with holes. Thus, the enhanced mobility can only be observed from the sample with n-type or intrinsic substrate. In other words, in spite of the fact that p-type substrate results in the best structural stability, it is unfavorable for electronic devices due to lack of enhancement in mobility. As for the growth on intrinsic substrate, although the highest electron mobility was obtained, its severe structural instability causes it to be unsuitable for CMOS applications. Thus, the growth on n-type Si(100) is better suit as it provides both substantial enhancement in electron mobility and satisfactory structural stability. The enhanced electron mobility at the Gd_2O_3(100)/n-type Si(100) interface was found to be in the range of 1676-1780 cm^2/Vs at room temperature with the sheet carrier concentration > 10^{13} cm^{-2}. Compared with heavily doped n-type substrates at the same carrier concentration, the mobility enhancement for the sample with n-type substrate could amount to a factor of four higher. This aspect of the enhanced mobility at the Gd_2O_3(100)/Si(100) interface could open up new possibilities in integration of high-κ materials into MOSFET applications.

REFERENCES

[1] K. K. N. Simon M. Sze, *Physics of Semiconductor Devices,* 3rd ed.: Wiley-Interscience, 2007.

[2] S. K. B. Ben G. Streetman, *Solid State Electronic Devices: International Edition*: Pearson Education, 2009.

[3] K. J. Yallup and D. J. Godfrey, "Shallow junction source/drain regions in CMOS/VLSI technologies," *Physica B+C,* vol. 129, pp. 269-274, 1985.

[4] R. Gwoziecki, T. Skotnicki, P. Bouillon, and P. Gentil, "Optimization of V-th roll-off in MOSFET's with advanced channel architecture - Retrograde doping and pockets," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 46, pp. 1551-1561, 1999.

[5] Y. Song, H. Zhou, and Q. Xu, "Source/drain technologies for the scaling of nanoscale CMOS device," *Solid State Sciences,* vol. 13, pp. 294-305, 2011.

[6] S. C. Song and J. W. Blatchford, "Review Paper: Advanced Source and Drain Technologies for Low Power CMOS at 22/20 nm Node and Below," *ELECTRONIC MATERIALS LETTERS,* vol. 7, pp. 277-285, 2011.

[7] (2012). *International Technology Roadmap for Semiconductors*. Available: http://www.itrs.net/Links/2011ITRS/Home2011.htm

[8] D. P. Norton, "Synthesis and properties of epitaxial electronic oxide thin-film materials," *Materials Science and Engineering: R: Reports,* vol. 43, pp. 139-247, 2004.

[9] J. Robertson, "High dielectric constant oxides," *The European Physical Journal - Applied Physics,* vol. 28, pp. 265-291, 2004.

[10] E. P. Gusev, V. Narayanan, and M. M. Frank, "Advanced high-k dielectric stacks with polySi and metal gates: Recent progress and current challenges," *IBM Journal of Research and Development,* vol. 50, pp. 387-410, 2006.

[11] H. J. Osten, A. Laha, E. Bugiel, D. Schwendt, and A. Fissel, "Growth of epitaxial lanthanide oxide based gate dielectrics," in *Signals, Circuits and Systems (SCS), 2009 3rd International Conference on*, 2009, pp. 1-6.

[12] H. J. Osten, A. Laha, M. Czernohorsky, E. Bugiel, R. Dargis, and A. Fissel, "Introducing crystalline rare-earth oxides into Si technologies," *physica status solidi (a),* vol. 205, pp. 695-707, 2008.

[13] M. Wu, Y. I. Alivov, and H. Morkoc, "High-k dielectrics and advanced channel concepts for Si MOSFET," *JOURNAL OF MATERIALS SCIENCE-MATERIALS IN ELECTRONICS,* vol. 19, pp. 915-951, 2008.

[14] J. Robertson and K. Xiong, "Electronic structure and band offsets of lanthanide oxides," *RARE EARTH OXIDE THIN FILMS: GROWTH, CHARACTERIZATION , AND APPLICATIONS,* vol. 106, pp. 313-329, 2007.

[15] J. H. Choi, Y. Mao, and J. P. Chang, "Development of hafnium based high-k materials—A review," *Materials Science and Engineering: R: Reports,* vol. 72, pp. 97-136, 2011.

[16] K. McKenna, A. Shluger, V. Iglesias, M. Porti, M. Nafr\, \#237, M. Lanza, and G. Bersuker, "Grain boundary mediated leakage current in polycrystalline HfO_2 films," *Microelectron. Eng.,* vol. 88, pp. 1272-1275, 2011.

[17] S. V. Ushakov, A. Navrotsky, Y. Yang, S. Stemmer, K. Kukli, M. Ritala, M. A. Leskelä, P. Fejes, A. Demkov, C. Wang, B. Y. Nguyen, D. Triyoso, and P. Tobin, "Crystallization in hafnia- and zirconia-based systems," *physica status solidi (b),* vol. 241, pp. 2268-2278, 2004.

[18] T. S. Böscke, S. Govindarajan, P. D. Kirsch, P. Y. Hung, C. Krug, B. H. Lee, J. Heitmann, U. Schröder, G. Pant, B. E. Gnade, and W. H. Krautschneider, "Stabilization of higher-κ tetragonal HfO_2 by SiO_2 admixture enabling thermally stable metal-insulator-metal capacitors," *Applied Physics Letters,* vol. 91, p. 072902, 2007.

[19] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Structural and electrical properties of HfLaOx films for an amorphous high-k gate insulator," *Applied Physics Letters,* vol. 89, p. 032903, 2006.

[20] W. J. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. P. Ma, "Effect of Al inclusion in HfO_2 on the physical and electrical properties of the dielectrics," *Electron Device Letters, IEEE,* vol. 23, pp. 649-651, 2002.

[21] J. Ni, Q. Zhou, Z. Li, and Z. Zhang, "Oxygen defect induced photoluminescence of HfO_2 thin films," *Applied Physics Letters,* vol. 93, p. 011905, 2008.

[22] D. Reicher, P. Black, and K. Jungling, "Defect Formation in Hafnium Dioxide Thin Films," *Appl. Opt.,* vol. 39, pp. 1589-1599, 2000.

[23] M. Modreanu, S. Monaghan, I. M. Povey, K. Cherkaoui, P. K. Hurley, and M. Androulidaki, "Investigation of bulk defects in amorphous and crystalline HfO_2 thin films," *Microelectron. Eng.,* vol. 88, pp. 1499-1502, 2011.

[24] G. Niu, *Epitaxy of Crystalline Oxides for Functional Materials Integration on Silicon*, 2010.

[25] M. Badylevich, S. Shamuilia, V. V. Afanas'ev, A. Stesmans, A. Laha, H. J. Osten, and A. Fissel, "Investigation of the electronic structure at interfaces of crystalline and amorphous Gd_2O_3 thin layers with silicon substrates of different orientations," *Applied Physics Letters,* vol. 90, pp. 252101-3, 2007.

[26] C. Merckling, G. Delhaye, M. El-Kazzi, S. Gaillard, Y. Rozier, L. Rapenne, B. Chenevier, O. Marty, G. Saint-Girons, M. Gendry, Y. Robach, and G. Hollinger, "Epitaxial growth of $LaAlO_3$ on Si(001) using interface engineering," *Microelectronics Reliability,* vol. 47, pp. 540-543, 2007.

[27] J. X. Wang, A. Laha, A. Fissel, D. Schwendt, R. Dargis, T. Watahiki, R. Shayduk, W. Braun, T. M. Liu, and H. J. Osten, "Crystal structure and strain state of molecular beam epitaxial grown Gd_2O_3 on Si(1 1 1) substrates: a diffraction study," *Semiconductor Science and Technology,* vol. 24, p. 045021, 2009.

[28] A. Fissel, R. Dargis, E. Bugiel, D. Schwendt, T. Wietler, J. Krügener, A. Laha, and H. J. Osten, "Single-crystalline Si grown on single-crystalline Gd_2O_3 by modified solid-phase epitaxy," *Thin Solid Films,* vol. 518, pp. 2546-2550, 2010.

[29] H. D. B. Gottlob, T. Echtermeyer, M. Schmidt, T. Mollenhauer, J. K. Efavi, T. Wahlbrink, M. C. Lemme, M. Czernohorsky, E. Bugiel, A. Fissel, H. J. Osten, and H. Kurz, "0.86-nm CET Gate Stacks With Epitaxial Gd_2O_3 High-k Dielectrics and FUSI NiSi Metal Electrodes," *Electron Device Letters, IEEE,* vol. 27, pp. 814-816, 2006.

[30] A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Q. Pan, R. Ramesh, and S. Salahuddin, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Applied Physics Letters,* vol. 99, 2011.

[31] T. N. Theis, "(Keynote) In Quest of a Fast, Low-Voltage Digital Switch," *ECS Transactions,* vol. 45, pp. 3-11, April 27, 2012 2012.

[32] S. Salahuddin and S. Dattat, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters,* vol. 8, pp. 405-410, 2008.

[33] N. Michael, G. Sonja, C. S. Dean, C. P. Stephen, and W. W. Graeme, "Density functional theory studies of the structure and electronic structure of pure and defective low index surfaces of ceria," *Surface Science,* vol. 576, pp. 217-229.

[34] N. Claudine, "Polar oxide surfaces," *Journal of Physics: Condensed Matter,* vol. 12, p. R367, 2000.

[35] G. Jacek, F. Fabio, and N. Claudine, "Polarity of oxide surfaces and nanostructures," *Reports on Progress in Physics,* vol. 71, p. 016501, 2008.

[36] A. Ohtomo and H. Y. Hwang, "A high-mobility electron gas at the $LaAlO_3/SrTiO_3$ heterointerface," *Nature,* vol. 427, pp. 423-426, 2004.

[37] W. Sitaputra and R. Tsu, "Enhancement in Electron Mobility at the Interface between Gd_2O_3(100) and n-type Si(100)," *ECS Transactions,* vol. 45, pp. 185-193, April 27, 2012 2012.

[38] W. J. Zhu, J. P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 51, pp. 98-105, 2004.

[39] (2007). *The Bixbyite (Mn_2O_3, $D5_3$) Structure*. Available: http://cst-www.nrl.navy.mil/lattice//struk/d5_3.html

[40] (2008). *The Fluorite (C1) Structure*. Available: http://cst-www.nrl.navy.mil/lattice//struk/c1.html

[41] C. G. Levi, "Metastability and microstructure evolution in the synthesis of inorganics from precursors," *Acta Materialia,* vol. 46, pp. 787-800, 1998.

[42] A. Laha, H. J. Osten, and A. Fissel, "Impact of Si substrate orientations on electrical properties of crystalline Gd2O3 thin films for high-K application," *Applied Physics Letters,* vol. 89, p. 143514, 2006.

[43] H. Osten, E. Bugiel, M. Czernohorsky, Z. Elassar, O. Kirfel, and A. Fissel, "Molecular Beam Epitaxy of Rare-Earth Oxides: Rare Earth Oxide Thin Films." vol. 106, M. Fanciulli and G. Scarel, Eds., ed: Springer Berlin / Heidelberg, 2007, pp. 101-114.

[44] T. Inoue, T. Ohsuna, L. Luo, X. D. Wu, C. J. Maggiore, Y. Yamamoto, Y. Sakurai, and J. H. Chang, "Growth of (110)-Oriented CeO_2 Layers on (100) Silicon Substrates," *Applied Physics Letters,* vol. 59, pp. 3604-3606, 1991.

[45] T. Schroeder, A. Giussani, J. Dabrowski, P. Zaumseil, H. J. Müssig, O. Seifarth, and P. Storck, "Engineered Si wafers: On the role of oxide heterostructures as buffers for the integration of alternative semiconductors," *physica status solidi (c),* vol. 6, pp. 653-662, 2009.

[46] A. Laha, E. Bugiel, J. X. Wang, Q. Q. Sun, A. Fissel, and H. J. Osten, "Effect of domain boundaries on the electrical properties of crystalline Gd_2O_3 thin films," *Applied Physics Letters,* vol. 93, p. 182907, 2008.

[47] Y. Jiang, J. B. Adams, and M. v. Schilfgaarde, "Density-functional calculation of CeO_2 surfaces and prediction of effects of oxygen partial pressure and temperature on stabilities," *The Journal of Chemical Physics,* vol. 123, p. 064701, 2005.

[48] K. N. Delfrey, *Rare Earths: Research and Applications*: Nova Science Publishers, 2008.

[49] N. V. Skorodumova, M. Baudin, and K. Hermansson, "Surface properties of CeO_2 from first principles," *Physical Review B,* vol. 69, 2004.

[50] M. Czernohorsky, E. Bugiel, H. J. Osten, A. Fissel, and O. Kirfel, "Impact of oxygen supply during growth on the electrical properties of crystalline Gd_2O_3 thin films on Si(001)," *Applied Physics Letters,* vol. 88, p. 152905, 2006.

[51] D. J. Dunstan, S. Young, and R. H. Dixon, "Geometrical theory of critical thickness and relaxation in strained-layer growth," *Journal of Applied Physics,* vol. 70, p. 3038, 1991.

[52] R. People and J. C. Bean, "Calculation of critical layer thickness versus lattice mismatch for GexSi1-x/Si strained-layer heterostructures," *Applied Physics Letters,* vol. 47, p. 322, 1985.

[53] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers. I. Misfit dislocations," *Journal of Crystal Growth,* vol. 27, pp. 118-125.

[54] P. W. Tasker, "The stability of ionic crystal surfaces," *Journal of Physics C: Solid State Physics,* vol. 12, p. 4977, 1979.

[55] J. Goniakowski and C. Noguera, "The concept of weak polarity: an application to the $SrTiO_3$(001) surface," *Surface Science,* vol. 365, pp. L657-L662, 1996.

[56] "ICDD-PDF4 (03-065-3181)," ed. International Centre for Data Diffraction, 2010.

[57] G. Herranz, M. Basletić, M. Bibes, C. Carrétéro, E. Tafra, E. Jacquet, K. Bouzehouane, C. Deranlot, A. Hamzić, J. M. Broto, A. Barthélémy, and A. Fert, "High Mobility in $LaAlO_3$/$SrTiO_3$ Heterostructures: Origin, Dimensionality, and Perspectives," *Physical Review Letters,* vol. 98, p. 216803, 2007.

[58] R. Pentcheva and W. E. Pickett, "Charge localization or itineracy at $LaAlO_3$/$SrTiO_3$ interfaces: Hole polarons, oxygen vacancies, and mobile electrons," *Physical Review B,* vol. 74, p. 035112, 2006.

[59] K. Yoshimatsu, R. Yasuhara, H. Kumigashira, and M. Oshima, "Origin of Metallic States at the Heterointerface between the Band Insulators $LaAlO_3$ and $SrTiO_3$," *Physical Review Letters,* vol. 101, p. 026802, 2008.

[60] M. Basletic, J. L. Maurice, C. Carrétéro, G. Herranz, O. Copie, M. Bibes, E. Jacquet, K. Bouzehouane, S. Fusil, and A. Barthélémy, "Mapping the spatial distribution of charge carriers in $LaAlO_3$/$SrTiO_3$ heterostructures," *Nature Materials,* vol. 7, pp. 621-625, 2008.

[61] B. K. Ridley, "Polarization-induced electron populations," *Applied Physics Letters*, vol. 77, pp. 990-992, 2000.

[62] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, pp. 3222-3233, 1999.

[63] C. Bell, S. Harashima, Y. Kozuka, M. Kim, B. G. Kim, Y. Hikita, and H. Y. Hwang, "Dominant Mobility Modulation by the Electric Field Effect at the $LaAlO_3/SrTiO_3$ Interface," *Physical Review Letters,* vol. 103, p. 226802, 2009.

[64] A. Brinkman, M. Huijben, M. van Zalk, J. Huijben, U. Zeitler, J. C. Maan, W. G. van der Wiel, G. Rijnders, D. H. A. Blank, and H. Hilgenkamp, "Magnetic effects at the interface between non-magnetic oxides," *Nat Mater,* vol. 6, pp. 493-496, 2007.

[65] K. Tse, D. Liu, K. Xiong, and J. Robertson, "Oxygen vacancies in high-k oxides," *Microelectronic Engineering,* vol. 84, pp. 2028-2031, 2007.

[66] M. V. Ganduglia-Pirovano, A. Hofmann, and J. Sauer, "Oxygen vacancies in transition metal and rare earth oxides: Current state of understanding and remaining challenges," *Surface Science Reports,* vol. 62, pp. 219-270, 2007.

[67] G. Pacchioni, "Oxygen Vacancy: The Invisible Agent on Oxide Surfaces," *ChemPhysChem,* vol. 4, pp. 1041-1047, 2003.

[68] T. Ami, Y. Ishida, N. Nagasawa, A. Machida, and M. Suzuki, "Room-temperature epitaxial growth of CeO_2(001) thin films on Si(001) substrates by electron beam evaporation," *Applied Physics Letters,* vol. 78, pp. 1361-1363, 2001.

[69] W. R. Thurber. (2011). *Hall Effect Measurements*. Available: http://www.nist.gov/pml/div683/hall.cfm

[70] A. L. Patterson, "The Scherrer Formula for X-Ray Particle Size Determination," *Physical Review,* vol. 56, pp. 978-982, 1939.

[71] D. A. W. Soares and C. A. Pimentel, "Precision interplanar spacing measurements of boron-doped silicon," *Journal of Applied Crystallography,* vol. 16, pp. 486-492, 1983.

APPENDIX A: CLASSIFICATION OF CRYSTAL SURFACES

Table A1. Classification of the main low-index crystal surface terminations [35]

Prototype Structure	Orientation	Surface Termination	Type	Tasker's Classification
(Rocksalt) NaCl	(1 0 0)	NaCl	Non-polar	I
(Rocksalt) NaCl	(1 1 0)	NaCl	Non-polar	I
(Rocksalt) NaCl	(1 1 1)	Na or Cl	Polar	III
(Fluorite) CaF_2	(1 0 0)	Ca or F_2	Polar	III
(Fluorite) CaF_2	(1 1 0)	CaF_2	Non-polar	I
(Fluorite) CaF_2	(1 1 1)	Ca/F/F… or F/F/Ca…	Polar	III
(Fluorite) CaF_2	(1 1 1)	F/Ca/F…	Non-polar	II
(Zinc blende) ZnS	(1 0 0)	Zn or S	Polar	III
(Zinc blende) ZnS	(1 1 0)	ZnS	Non-polar	I
(Zinc blende) ZnS	(1 1 1)	Zn or S	Polar	III
(Wurtzite) ZnO	(0 0 0 1)	Zn or O	Polar	III
Rutile TiO_2	(1 0 0)	Ti or O	Polar	III
Rutile TiO_2	(1 1 0)	O	Non-polar	II
Rutile TiO_2	(1 1 0)	Ti or O/O	Polar	II
Rutile TiO_2	(0 0 1)	TiO_2	Non-polar	I
Cu_2O	(1 0 0)	O or Cu_2	Polar	III
Cu_2O	(1 1 0)	CuO or Cu	Polar	III
Cu_2O	(1 1 1)	O/Cu_4/O…	Non-polar	II
Cu_2O	(1 1 1)	Cu_4/O.. or O/O/Cu_4…	Polar	II
ReO_3	(1 0 0)	O or ReO_2	Polar	III
ReO_3	(1 1 0)	ReO or O_2	Polar	III
ReO_3	(1 1 1)	Re or O_3	Non-polar	III
(Cristobalite) β-SiO_2	(1 0 0)	Si or O_2	Polar	III
(Cristobalite) β-SiO_2	(1 1 1)	O or Si or O_3	Polar	III
(Corundum) α-Al_2O_3	(0 0 0 1)	Al/O_3/Al…	Non-polar	II
(Corundum) α-Al_2O_3	(0 0 0 1)	O_3/Al.. or Al/Al/O_3..	Polar	II
(Spinel) $MgAl_2O_4$	(1 0 0)	Mg or O_2 or Al_2	Polar	III
(Spinel) $MgAl_2O_4$	(1 1 0)	$MgAlO_2$ or O or Al	Polar	III
(Spinel) $MgAl_2O_4$	(1 1 1)	Mg or Al or O_3 or O Al_3	Polar	III
(Cubic) $BaTiO_3$	(1 0 0)	BaO or TiO_2	Polar	I
(Cubic) $BaTiO_3$	(1 1 0)	O_2 or BaTiO	Polar	III
(Cubic) $BaTiO_3$	(1 1 1)	BaO_3 or Ti	Polar	III

APPENDIX B: POWDER DIFFRACTION FILES

03-065-3181 Jul 12, 2012 1:44 PM (icdd)

Status Alternate **QM:** Indexed (I) **Pressure/Temperature:** Ambient **Chemical Formula:** Gd2 O3
Empirical Formula: Gd2 O3 **Weight %:** Gd86.76 O13.24 **Atomic %:** Gd40.00 O60.00
Compound Name: Gadolinium Oxide

Radiation: CuKá1 **λ:** 1.5406Å **d-Spacing:** Calculated **Intensity:** Calculated **I/Ic:** 12.65

SYS: Cubic **SPGR:** Ia-3 (206)
Author's Cell [AuthCell a: 10.818Å **AuthCell Vol:** 1266.02Å³ **AuthCell Z:** 16.00 **AuthCell MolVol:** 79.13 **]**
Dcalc: 7.607g/cm³ **Dstruc:** 7.61g/cm³ **SS/FOM:** F(30) = 999.9(0.0000, 30)

Space Group: Ia-3 (206) **Molecular Weight:** 362.50
Crystal Data [XtlCell a: 10.818Å **XtlCell b:** 10.818Å **XtlCell c:** 10.818Å **XtlCell α:** 90.00° **XtlCell β:** 90.00°
XtlCell γ: 90.00° **XtlCell Vol:** 1266.02Å³ **XtlCell Z:** 16.00 **]**
Crystal Data Axial Ratio [a/b: 1.000 **c/b:** 1.000 **]**
Reduced Cell [RedCell a: 9.369Å **RedCell b:** 9.369Å **RedCell c:** 9.369Å **RedCell α:** 109.47°
RedCell β: 109.47° **RedCell γ:** 109.47° **RedCell Vol:** 633.01Å³ **]**

TDP Type: B **Crystal (Symmetry Allowed):** Centrosymmetric

SG Symmetry Operators:

Seq	Operator	Seq	Operator	Seq	Operator	Seq	Operator	Seq	Operator	Seq	Operator
1	x,y,z	5	-x+1/2,y,-z	9	z,x,y	13	-z+1/2,x,-y	17	y,z,x	21	-y+1/2,z,-x
2	-x,-y,-z	6	x+1/2,-y,z	10	-z,-x,-y	14	z+1/2,-x,y	18	-y,-z,-x	22	y+1/2,-z,x
3	x,-y,-z+1/2	7	-x,-y+1/2,z	11	z,-x,-y+1/2	15	-z,-x+1/2,y	19	y,-z,-x+1/2	23	-y,-z+1/2,x
4	-x,y,z+1/2	8	x,y+1/2,-z	12	-z,x,y+1/2	16	z,x+1/2,-y	20	-y,z,x+1/2	24	y,z+1/2,-x

Atomic Coordinates:

Atom	Num	Wyckoff	Symmetry	x	y	z	SOF	IDP	AET
Gd	1			0.97	0.0	0.25	1.0	0.5	
Gd	2			0.25	0.25	0.25	1.0	0.5	
O	3			0.385	0.145	0.38	1.0	0.5	

Pearson: cI80.00 **Prototype Structure:** Mn Fe O3 **Prototype Structure (Alpha Order):** Fe Mn O3
LPF Prototype Structure: (Mn0.5 Fe0.5)2 O3,cI80,206 **LPF Prototype Structure (Alpha Order):** Fe Mn O3
Subfile(s): Inorganic, Common Phase, Alternate Pattern, Metals & Alloys, Superconducting Material, NIST Pattern
Entry Date: 02/11/2005 **Last Modification Date:** 01/26/2011

Cross-Ref PDF #'s: 00-012-0797 (Primary), 00-043-1014 (Primary), 01-073-2652 (Alternate), 01-074-3085 (Alternate), 01-076-8040 (Alternate), 01-078-3798 (Alternate), 01-086-2477 (Alternate), ✓ 04-003-4699 (Alternate), ✓ 04-003-5831 (Alternate), ✓ 04-004-1606 (Alternate), ✓ 04-004-5972 (Alternate), ✓ 04-004-8970 (Alternate), ✓ 04-005-4776 (Alternate), ✓ 04-005-8062 (Alternate), ✓ 04-006-2387 (Alternate), ✓ 04-006-4362 (Alternate), ✓ 04-006-7291 (Alternate), ✓ 04-010-0033 (Alternate), ✓ 04-010-3292 (Primary), ✓ 04-012-8039 (Alternate), ✓ 04-015-1513 (Alternate)

References:

Type	Reference
Primary Reference	Calculated from NIST using POWD-12++.
Structure	H.Bommer Z. Anorg. Allg. Chem. 241, 273 (1939).

Database Comments: Additional Patterns: See PDF 01-086-2477. NIST M&A collection code: N AL4315 4588. Temperature Factor: IB=Gd,O. Minor Warning: No e.s.d reported/abstracted on the cell dimension. No Rfactor reported/abstracted.

d-Spacings (82) - 03-065-3181 (Fixed Slit Intensity) - Cu Kα1 1.54056Å

2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*
16.3743	5.409000	2	2	0	0		53.5297	1.710480	7	0	2	6		76.7401	1.240910	60	6	6	2	
20.0889	4.416430	110	2	1	1		54.9618	1.669250	28	1	4	5		77.9309	1.224900	1	7	5	2	
23.2370	3.824740	1	2	2	0		56.3690	1.630870	256	6	2	2		79.1167	1.209490	41	0	4	8	
28.5595	**3.122890**	999	2	2	2		57.7532	1.595030	44	1	3	6		80.2976	1.194650	7	8	3	3	
30.9026	2.891230	14	1	2	3		59.1173	1.561440	48	4	4	4		81.4746	1.180340	6	2	4	8	
33.0955	**2.704500**	311	4	0	0		60.4615	1.529900	15	5	4	3		82.6482	1.166530	14	9	2	1	
35.1664	2.549830	46	4	1	1		61.7885	1.500190	7	0	4	6		83.8181	1.153200	1	6	6	4	
37.1362	2.418980	7	4	2	0		63.0994	1.472140	20	6	3	3		84.9851	1.140320	15	1	5	8	
39.0203	2.306410	30	3	3	2		64.3947	1.445620	9	6	4	2		87.3148	1.115790	13	7	6	3	
40.8310	2.208210	6	4	2	2		68.2024	1.373890	18	1	5	6		88.4772	1.104110	40	8	4	4	
42.5776	2.121580	65	1	3	4		69.4486	1.352250	34	8	0	0		89.6399	1.092780	14	8	5	3	
45.9087	1.975090	15	1	2	5		70.6849	1.331600	25	8	1	1		90.8015	1.081800	7	8	6	0	
47.5052	**1.912370**	353	4	4	0		71.9111	1.311880	11	8	2	0		91.9640	1.071140	5	10	1	1	
49.0619	1.855270	17	4	3	3		73.1295	1.293000	14	3	5	6		93.1272	1.060790	16	2	6	8	
50.5827	1.803000	3	6	0	0		74.3403	1.274910	8	8	2	2		94.2910	1.050740	4	3	4	9	
52.0711	1.754910	36	6	1	1		75.5431	1.257570	23	8	3	1		95.4579	1.040960	32	10	2	2	

00-005-0565 Jul 12, 2012 1:59 PM (icdd)

Status Alternate **QM:** Star (S) **Pressure/Temperature:** Ambient **Chemical Formula:** Si **Empirical Formula:** Si
Weight %: Si100.00 **Atomic %:** Si100.00 **Compound Name:** Silicon **Mineral Name:** Silicon, syn (NR)

Radiation: CuKá1 **λ:** 1.5405Å **Filter:** Ni Beta **Intensity:** Diffractometer **I/Ic:** 4.7

SYS: Cubic **SPGR:** Fd-3m (227)
Author's Cell [AuthCell a: 5.4301Å **AuthCell Vol:** 160.11Å³ **AuthCell Z:** 8.00 **AuthCell MolVol:** 20.01 **]**
Dcalc: 2.33g/cm³ **SS/FOM:** F(11) = 61.6(0.0137, 13)

Space Group: Fd-3m (227) **Molecular Weight:** 28.09
Crystal Data [XtlCell a: 5.430Å **XtlCell b:** 5.430Å **XtlCell c:** 5.430Å **XtlCell α:** 90.00° **XtlCell β:** 90.00°
XtlCell γ: 90.00° **XtlCell Vol:** 160.11Å³ **XtlCell Z:** 8.00 **]** **Crystal Data Axial Ratio [a/b:** 1.000 **c/b:** 1.000 **]**
Reduced Cell [RedCell a: 3.840Å **RedCell b:** 3.840Å **RedCell c:** 3.840Å **RedCell α:** 60.00°
RedCell β: 60.00° **RedCell γ:** 60.00° **RedCell Vol:** 40.03Å³ **]**

Crystal (Symmetry Allowed): Centrosymmetric

CAS: 7440-21-3 **Pearson:** cF8.00 **Prototype Structure:** C **Prototype Structure (Alpha Order):** C
LPF Prototype Structure: C,cF8,227 **LPF Prototype Structure (Alpha Order):** C

Subfile(s): Alternate Pattern, Ceramic (Semiconductor), Forensic, Inorganic, NBS Pattern, Common Phase, Metals & Alloys, Mineral Related (Mineral , Synthetic)

Last Modification Date: 01/11/2011

Cross-Ref PDF #'s: 00-001-0787 (Deleted), 00-001-0791 (Deleted), 00-002-0561 (Deleted), 00-003-0529 (Deleted), 00-026-1481 (Alternate), 00-027-1402 (Primary), 01-070-5680 (Alternate), 01-070-8272 (Alternate), 01-071-3770 (Alternate), 01-071-4631 (Alternate), 01-073-6978 (Alternate), 01-075-0589 (Alternate), 01-077-2108 (Alternate), 01-077-2109 (Alternate), 01-077-2110 (Alternate), 01-077-2111 (Alternate), 01-089-2749 (Alternate), 01-089-2955 (Alternate), ✓ 03-065-1060 (Alternate), ✓ 04-001-7247 (Primary), ✓ 04-002-0118 (Alternate), ✓ 04-002-0891 (Alternate), ✓ 04-002-2831 (Alternate), ✓ 04-003-1456 (Alternate), ✓ 04-003-3352 (Alternate), ✓ 04-003-3353 (Alternate), ✓ 04-003-4734 (Alternate), ✓ 04-004-5099 (Alternate), ✓ 04-004-6896 (Alternate), ✓ 04-005-9699 (Alternate), ✓ 04-006-2527 (Alternate), ✓ 04-006-2591 (Alternate), ✓ 04-006-4528 (Alternate), ✓ 04-006-6436 (Alternate), ✓ 04-007-5232 (Alternate), ✓ 04-007-8736 (Alternate), ✓ 04-010-2410 (Alternate), ✓ 04-012-0806 (Alternate), ✓ 04-012-7888 (Alternate), ✓ 04-013-4795 (Alternate), ✓ 04-014-0211 (Alternate), ✓ 04-014-0247 (Alternate), ✓ 04-014-8844 (Alternate)

References:

Type	Reference
Primary Reference	Swanson, Fuyat. Natl. Bur. Stand. (U. S.), Circ. 539 II, 6 (1953).

Database Comments: Additional Patterns: See PDF 00-027-1402. Analysis: Spectroscopic analysis: <0.001% Cu, Ag, Zn, Sn, Mg, Fe. Color: Black, gray. Sample Source or Locality: Sample from Johnson Matthey Company. Temperature of Data Collection: Pattern taken at 299 K. Unit Cell Data Source: Powder Diffraction.

d-Spacings (11) - 00-005-0565 (Fixed Slit Intensity) - Cu Kα1 1.54056Å

2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*
28.4190	**3.138000**	100	1	1	1		76.3699	1.246000	13	3	3	1		114.1258	0.917800	11	5	3	1	
47.3049	**1.920000**	60	2	2	0		88.0561	1.108300	17	4	2	2		127.5680	0.858600	9	6	2	0	
56.1019	**1.638000**	35	3	1	1		94.9716	1.045000	9	5	1	1		136.9250	0.828100	5	5	3	3	
69.1709	1.357000	8	4	0	0		106.7311	0.959900	5	4	4	0								

00-050-1529 Aug 1, 2012 3:50 PM (icdd)

Status Primary **QM:** Star (S) **Pressure/Temperature:** Ambient **Chemical Formula:** Gd Si
Empirical Formula: Gd Si **Weight %:** Gd84.85 Si15.15 **Atomic %:** Gd50.00 Si50.00
Compound Name: Gadolinium Silicon

Radiation: CuKá1 **λ:** 1.5406Å **Filter:** Ni Beta **d-Spacing:** Diff. **Cutoff:** 14.70 **Intensity:** Diffractometer

SYS: Orthorhombic **SPGR:** Pnma (62)
Author's Cell [AuthCell a: 7.9827(3)Å **AuthCell b:** 3.8591(1)Å **AuthCell c:** 5.7445(2)Å **AuthCell Vol:** 176.97Å³
AuthCell Z: 4.00 **AuthCell MolVol:** 44.24] **Author's Cell Axial Ratio [c/a:** 0.720 **a/b:** 2.069 **c/b:** 1.489]
Dcalc: 6.956g/cm³ **SS/FOM:** F(30) = 130.5(0.0070, 33)

Space Group: Pbnm (62) **Molecular Weight:** 185.34
Crystal Data [XtlCell a: 5.744Å **XtlCell b:** 7.983Å **XtlCell c:** 3.859Å **XtlCell α:** 90.00° **XtlCell β:** 90.00°
XtlCell γ: 90.00° **XtlCell Vol:** 176.97Å³ **XtlCell Z:** 4.00]
Crystal Data Axial Ratio [c/a: 0.672 **a/b:** 0.720 **c/b:** 0.483]
Reduced Cell [RedCell a: 3.859Å **RedCell b:** 5.744Å **RedCell c:** 7.983Å **RedCell α:** 90.00°
RedCell β: 90.00° **RedCell γ:** 90.00° **RedCell Vol:** 176.97Å³]

Crystal (Symmetry Allowed): Centrosymmetric

Pearson: oP8.00 **Prototype Structure:** Fe B **Prototype Structure (Alpha Order):** B Fe
LPF Prototype Structure: Fe B-b,oP8,62 **LPF Prototype Structure (Alpha Order):** B Fe
Subfile(s): Metals & Alloys, Inorganic, Primary Pattern **Entry Date:** 06/15/1999 **Last Modification Date:** 01/12/2011
Cross-Ref PDF #'s: ✓ 04-003-0953 (Alternate), ✓ 04-003-2107 (Primary), ✓ 04-004-0796 (Alternate), ✓ 04-004-0988 (Alternate), ✓ 04-004-1703 (Alternate), ✓ 04-004-3492 (Alternate), ✓ 04-004-4033 (Alternate)

References:

Type	Reference
Primary Reference	Pecharsky, V., Akselrud, L., Davydov, V., L`viv Inst. of Theoretical Material Research, Ukraine. ICDD Grant-in-Aid (1998).

Database Comments: Additional Patterns: See PDF 01-080-0705. Color: Metallic. Sample Preparation: Prepared by arc melting of constituents under argon, annealed at 1070 K for 280 hours in an evacuated, sealed quartz tube, followed by quenching into cold water. Temperature of Data Collection: Pattern taken at 295 K. Unit Cell Data Source: Powder Diffraction.

d-Spacings (80) - 00-050-1529 (Fixed Slit Intensity) - Cu Kα1 1.54056Å

2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*
19.0175	4.662760	8	1	0	1		57.5024	1.601390	1	0	2	2		79.6426	1.202820	5	5	2	1	
22.2594	3.990450	21	2	0	0		58.5214	1.575910	18	2	1	3		79.7866	1.201010	<1	3	1	4	
27.1883	3.277190	27	2	0	1		58.7464	1.570410	36	1	2	2		80.0605	1.197590	6	2	3	1	
27.8302	3.203040	32	0	1	1		59.4152	1.554320	7	3	0	3		82.4758	1.168530	4	5	1	3	
30.0322	**2.973020**	100	1	1	1		60.1011	1.538210	3	5	0	1		83.0765	1.161600	8	1	3	2	
31.1422	2.869530	3	0	0	2		61.4644	1.507320	25	3	2	1		83.9172	1.152090	13m	0	2	4	
32.2381	**2.774440**	84	2	1	0		62.4462	1.485960	3	2	2	2		83.9172	1.152090	m	6	1	2	
33.1221	**2.702390**	80	1	0	2		64.5870	1.441780	1	3	1	3		84.9649	1.140540	1	1	2	4	
35.9210	2.497980	48	2	1	1		64.8731	1.436110	12	0	0	4		85.4465	1.135340	1	3	3	1	
37.2110	2.414290	51	3	0	1		65.2410	1.428900	11	5	1	1		85.8862	1.130650	5	5	2	2	
38.5960	2.330780	<1	2	0	2		66.0708	1.412950	2	1	0	4		86.5726	1.123440	13	4	2	3	
40.7258	2.213670	45	1	1	2		67.0073	1.395460	3	5	0	2		87.3011	1.115930	7	4	1	4	
44.2058	2.047140	6	3	1	1		67.7727	1.381550	16	4	0	3		88.2013	1.106850	2	2	2	4	
45.4387	1.994420	1m	4	0	0		69.4868	1.351600	2	2	0	4		88.4681	1.104200	2	2	0	5	
45.4387	1.994420	m	2	1	2		69.6690	1.348510	15	4	2	1		89.3906	1.095180	4	6	2	0	
47.0537	1.929660	31	0	2	0		70.2262	1.339170	<1	1	2	3		89.8405	1.090860	5	1	1	5	
48.2398	1.884950	21	4	0	1		70.7350	1.330780	7	6	0	0		90.8553	1.081300	4	4	3	0	
48.8995	1.861050	2	1	0	3		71.8826	1.312330	16	5	1	2		91.6179	1.074280	12m	7	1	1	
51.1976	1.782780	2	1	2	1		73.5495	1.286650	5	2	2	3		91.6179	1.074280	m	3	3	2	
51.5175	1.772460	20	4	1	0		74.3048	1.275430	13	2	1	4		92.3501	1.067670	3m	0	3	3	
52.4905	1.741870	37	3	1	2		75.5304	1.257750	4	6	1	0		92.3501	1.067670	m	5	0	4	
52.6496	1.736980	5	2	2	0		75.7336	1.254880	3	0	3	1		93.0679	1.061310	2	2	1	5	
53.0026	1.726240	9	2	0	3		76.8067	1.240000	9	1	3	1		93.2266	1.059920	8	7	0	2	
53.3704	1.715210	15	0	1	3		77.6468	1.228670	6	6	1	1		93.3894	1.058500	2	1	3	3	
54.1023	1.693720	3	4	1	1		77.8183	1.226390	2	5	0	3		93.8225	1.054750	4	3	0	5	
54.6854	1.677030	12	1	1	3		77.9717	1.224360	7	2	3	0		94.2123	1.051410	5	6	1	3	
55.1913	1.662850	11	2	2	1		79.0385	1.210490	7	3	2	3								

01-077-4755 Jul 31, 2012 10:52 AM (icdd)

Status Alternate **QM:** Star (S) **Pressure/Temperature:** Ambient **Chemical Formula:** Gd5 Si4
Empirical Formula: Gd5 Si4 **Weight %:** Gd87.50 Si12.50 **Atomic %:** Gd55.56 Si44.44 **ANX:** N4O5
Compound Name: Gadolinium silicide

Radiation: CuKá1 **λ:** 1.5406Å **d-Spacing:** Calculated **Intensity:** Calculated **I/Ic:** 3.08

SYS: Orthorhombic **SPGR:** Pnma (62)
Author's Cell [AuthCell a: 7.4823(18)Å **AuthCell b:** 14.7380(40)Å **AuthCell c:** 7.7460(18)Å
AuthCell Vol: 854.18Å³ **AuthCell Z:** 4.00 **AuthCell MolVol:** 213.54]
Author's Cell Axial Ratio [c/a: 1.035 **a/b:** 0.508 **c/b:** 0.526] **Dcalc:** 6.987g/cm³ **Dstruc:** 6.99g/cm³
SS/FOM: F(30) = 999.9(0.0005, 32) **R-factor:** 0.033

Space Group: Pcmn (62) **Molecular Weight:** 898.59
Crystal Data [XtlCell a: 7.746Å **XtlCell b:** 14.738Å **XtlCell c:** 7.482Å **XtlCell α:** 90.00° **XtlCell β:** 90.00°
XtlCell γ: 90.00° **XtlCell Vol:** 854.18Å³ **XtlCell Z:** 4.00]
Crystal Data Axial Ratio [c/a: 0.966 **a/b:** 0.526 **c/b:** 0.508]
Reduced Cell [RedCell a: 7.482Å **RedCell b:** 7.746Å **RedCell c:** 14.738Å **RedCell α:** 90.00°
RedCell β: 90.00° **RedCell γ:** 90.00° **RedCell Vol:** 854.18Å³]

Crystal (Symmetry Allowed): Centrosymmetric

Pearson: oP36.00 **Prototype Structure:** Sm5 Ge4 **Prototype Structure (Alpha Order):** Ge4 Sm5
Subfile(s): ICSD Pattern, Inorganic, Alternate Pattern, Metals & Alloys **Entry Date:** 11/13/2009
Last Modification Date: 01/19/2011

Cross-Ref PDF #'s: 01-078-7316 (Alternate), ✓ 04-004-3341 (Alternate), ✓ 04-006-3314 (Alternate), ✓ 04-007-1188 (Alternate), ✓ 04-008-5156 (Primary), ✓ 04-013-1587 (Alternate), ✓ 04-013-1588 (Alternate), ✓ 04-013-4008 (Alternate), ✓ 04-015-0546 (Alternate)

References:

Type	Reference
Primary Reference	Calculated from ICSD using POWD-12++.
Structure	"Gd5-x Yx Tt4 (Tt = Si or Ge): Effect of metal substitution on structure, bonding, and magnetism". Misra Sumohan, Miller G.J. J. Am. Chem. Soc. 130, 13900 (2008).

Database Comments: ANX: N4O5. Analysis: Gd5 Si4. Formula from original source: Gd5 Si4. ICSD Collection Code: 249771 FIZ249771. Calculated Pattern Original Remarks: Tt=Si; x=0. For concentration series see CCodes 249771-249775. Temperature of Data Collection: 298 K. Wyckoff Sequence: d3 c3 (PNMA). Unit Cell Data Source: Single Crystal.

d-Spacings (198) - 01-077-4755 (Fixed Slit Intensity) - Cu Kα1 1.54056Å

2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*	2θ	d(Å)	I	h	k	l	*
12.0002	7.369000	33	0	2	0		34.6697	2.585220	210	1	5	1		44.5595	2.031710	m	0	7	1	
12.9005	6.856650	10	0	1	1		35.4865	2.527560	19	2	2	2		44.9056	2.016850	2	3	2	2	
16.4583	5.381600	23	1	0	1		35.6805	2.514260	285	1	4	2		45.3305	1.998930	5m	1	6	2	
17.5293	5.055120	30	1	1	1		36.0964	2.486240	69	2	4	1		45.3305	1.998930	m	3	4	1	
20.4178	4.346020	89	1	2	1		36.5514	2.456330	239	0	6	0		45.6111	1.987280	27m	2	6	1	
21.4004	4.148650	13	0	3	1		36.7929	2.440760	169	1	0	3		45.6111	1.987280	m	2	5	2	
22.9435	3.873000	92	0	0	2		37.3124	2.407960	334	1	1	3		46.2646	1.960720	2	1	7	1	
23.7637	3.741150	4	2	0	0		37.8652	2.374070	342	3	0	1		46.5243	1.950380	5	2	3	3	
24.1345	3.684500	223	0	4	0		38.0999	2.359980	24	2	3	2		46.7313	1.942220	3	0	5	3	
24.5144	3.628260	181m	1	3	1		38.3724	2.343850	71	3	1	1		46.8776	1.936500	1	0	0	4	
24.5144	3.628260	m	2	1	0		38.8642	2.315310	187m	1	2	3		47.0817	1.928580	1	3	3	2	
25.8822	3.439530	261	1	0	2		38.8642	2.315310	m	2	5	0		48.5196	1.874730	81m	1	0	4	
25.9682	3.428330	187	0	2	2		39.3910	2.285550	10	0	3	3		48.5196	1.874730	m	0	2	4	
26.4363	3.368810	54	2	0	1		39.8608	2.259690	17	3	2	1		48.9362	1.859740	124	1	1	4	
26.5902	3.349530	213	1	1	2		40.2606	2.238170	16m	1	5	2		49.2413	1.848930	15	3	5	1	
26.7011	3.335870	78	2	2	0		40.2606	2.238170	m	1	6	1		49.4318	1.842250	106m	0	8	0	
27.1299	3.284110	458	2	1	1		40.6365	2.218330	50	2	5	1		49.4318	1.842250	m	2	4	3	
28.6170	3.116740	3	1	2	2		41.2676	2.185850	4	1	3	3		49.6455	1.834820	27	2	7	0	
29.1220	3.063830	14	2	2	1		41.5227	2.173010	1	2	4	2		50.1272	1.818310	151m	4	0	1	
29.3532	3.040220	118	1	4	1		42.2440	2.137560	3	3	3	1		50.1272	1.818310	m	1	2	4	
29.9977	2.976360	467	2	3	0		42.5051	2.125030	2	2	0	3		50.2507	1.814130	59m	2	6	2	
31.7312	**2.817600**	652	1	3	2		42.9663	2.103280	44	2	1	3		50.2507	1.814130	m	4	2	0	
32.1919	**2.778320**	999	2	3	1		43.1032	2.096920	11	3	0	2		50.5341	1.804620	28	4	1	1	
32.4733	2.754880	125	0	5	1		43.5594	2.076010	7m	3	1	2		50.8584	1.793870	105m	1	7	2	
33.2689	2.690800	37	2	0	2		43.5594	2.076010	m	0	6	2		50.8584	1.793870	m	3	0	3	
33.5423	**2.669490**	695	0	4	2		44.0660	2.053310	36	2	6	0		51.1164	1.785420	141	2	7	1	
33.8353	2.647040	435	2	1	2		44.3269	2.041830	4	2	2	3		51.2611	1.780720	22	3	1	3	
34.1263	2.625130	17	2	4	0		44.5595	2.031710	4m	1	4	3		51.7399	1.765360	6	4	2	1	